ISSCC 2013 Plenary Session

Continuing to Shrink: Next-Generation Lithography- Progress and Prospects

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Veldhoven, The Netherlands

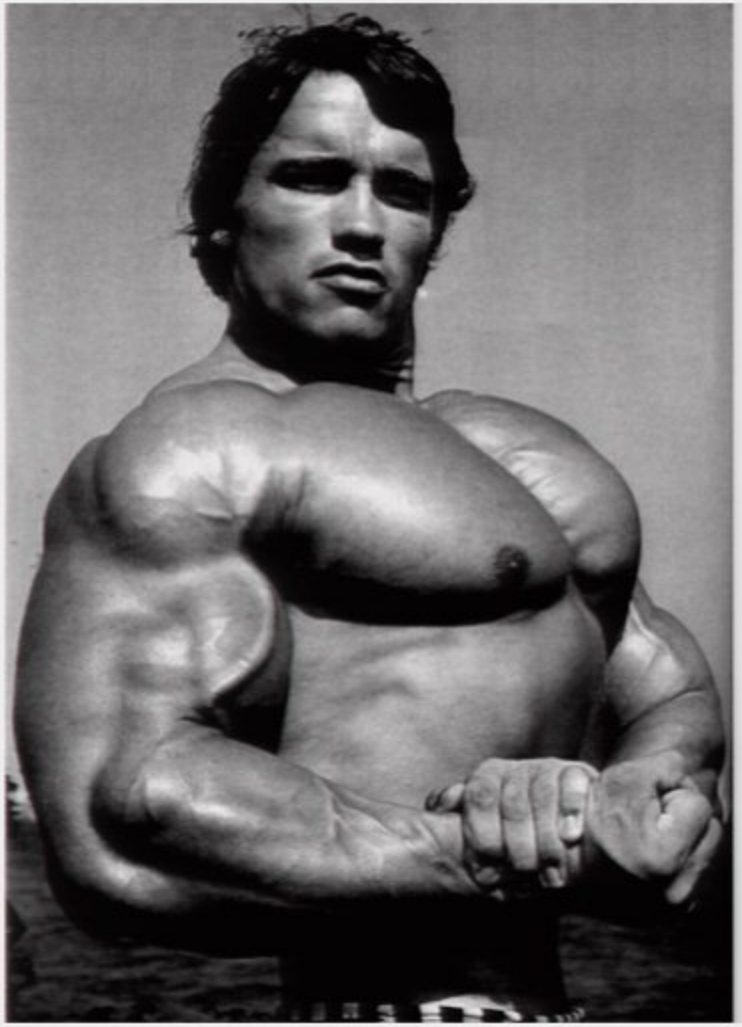
ASML

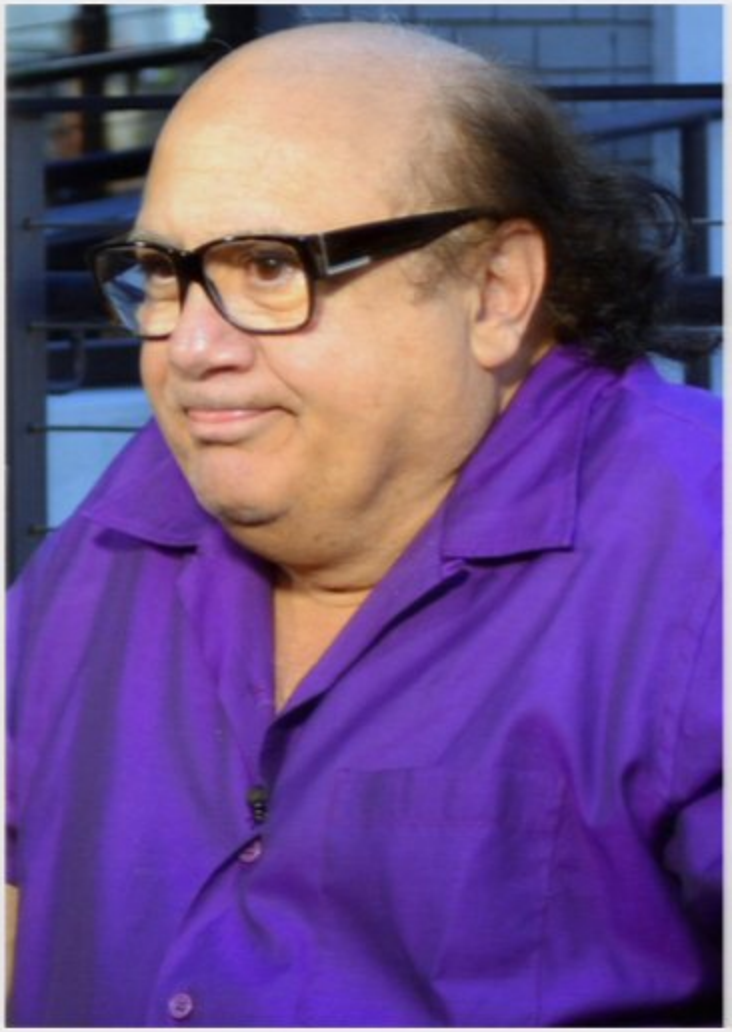
Continuing to shrink: Next generation lithography - progress and prospects

Martin van den Brink

ISSCC Conference 2013, San Francisco

We couldn't be more different…





… but we have a joint challenge

Scaling is needed for **lower cost** with improved performance. Affordable scaling in lithography can be achieved:

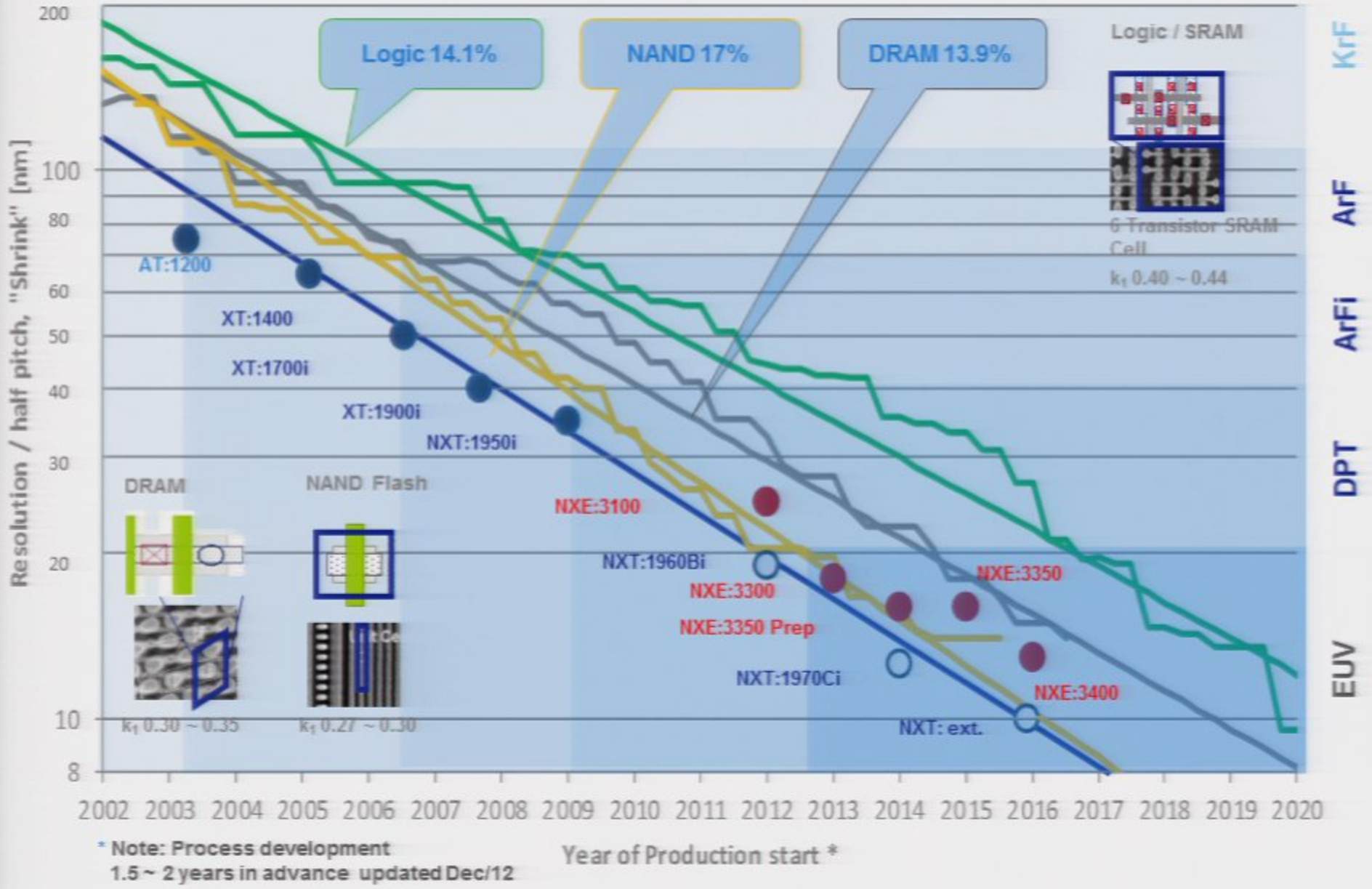
- Drive **productivity and yield (overlay) using immersion lithography** in combination with double patterning
- Seek disruptive, more scalable and cost reduction opportunities:
  - **EUV**
  - **450mm**

Agenda

- **Shrink roadmap**
- Holistic Lithography on immersion platform
- EUV lithography
- 450 mm
- Future

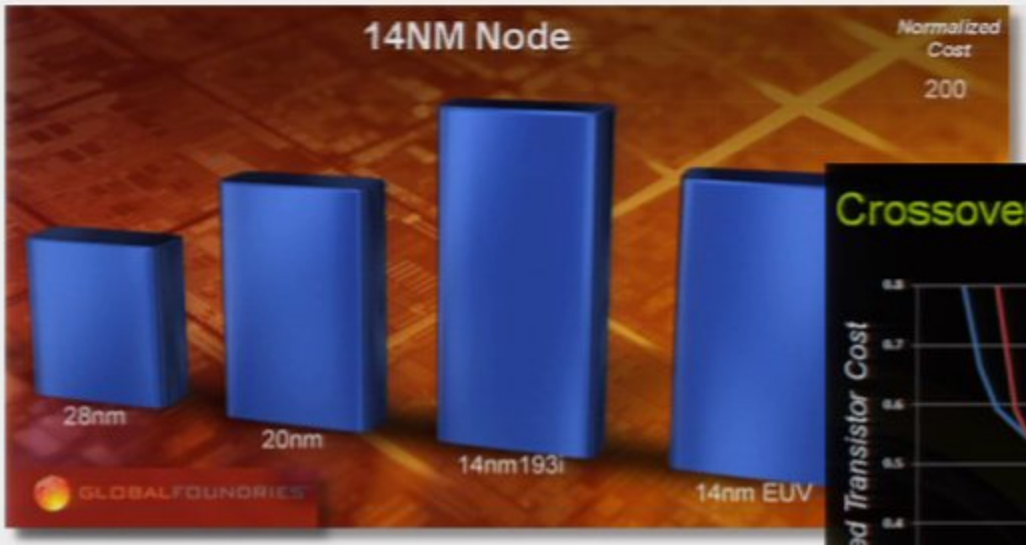
Industry roadmap towards < 10 nm resolution

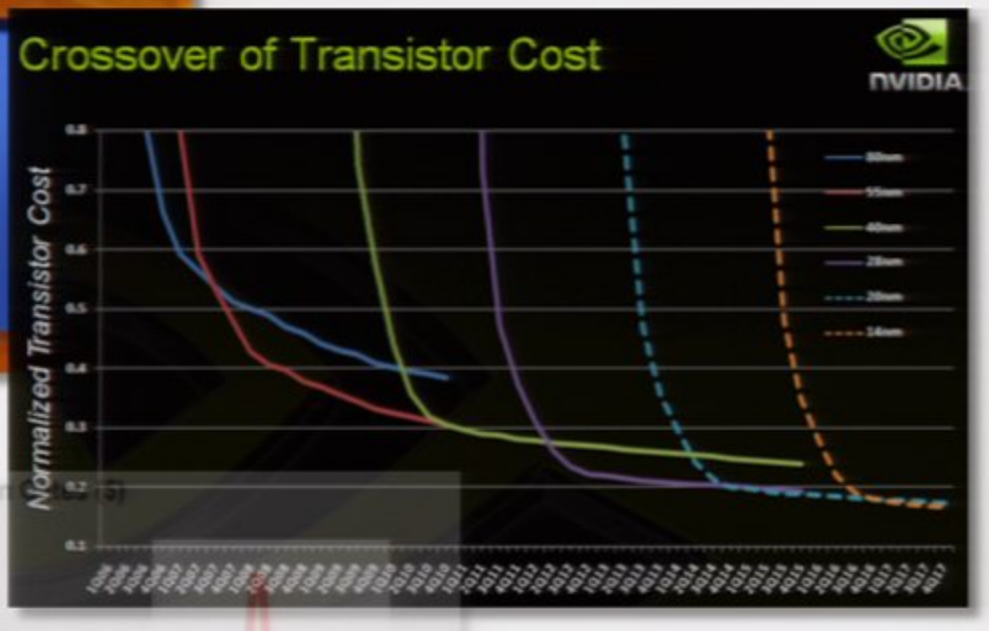
Lithography supports shrink roadmap

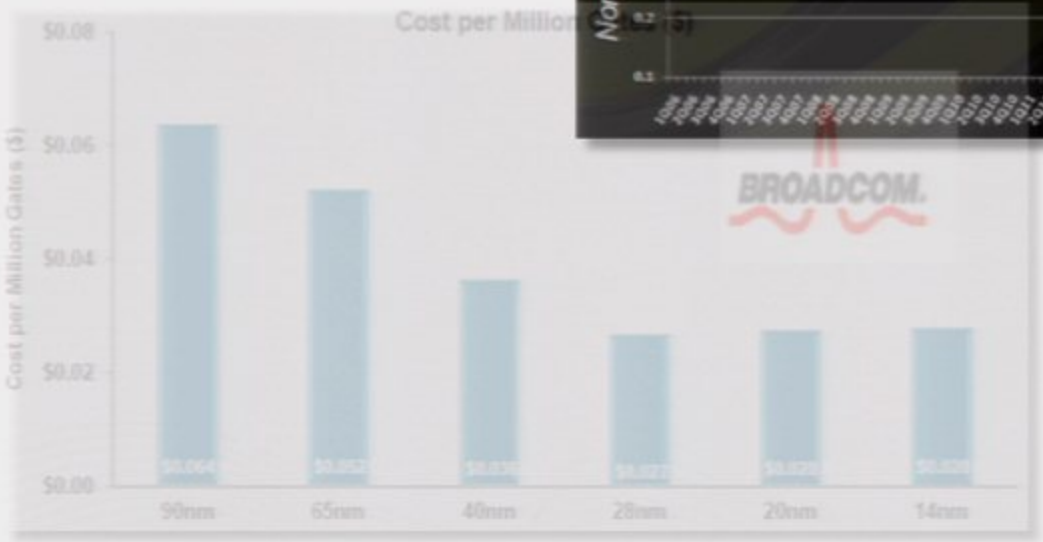


* Note: Process development
1.5 ~ 2 years in advance updated Dec/12

Cost becomes a concern post 28 nm

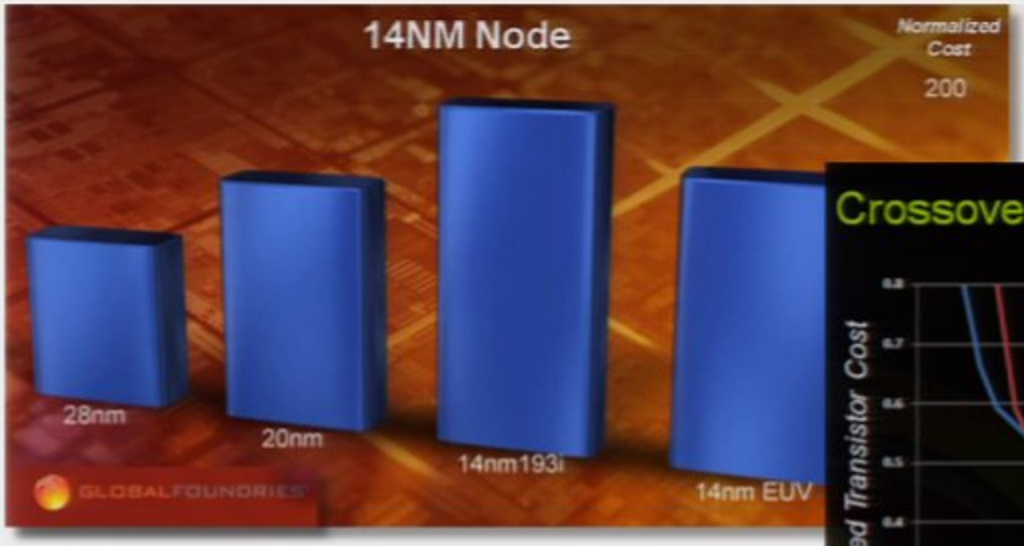


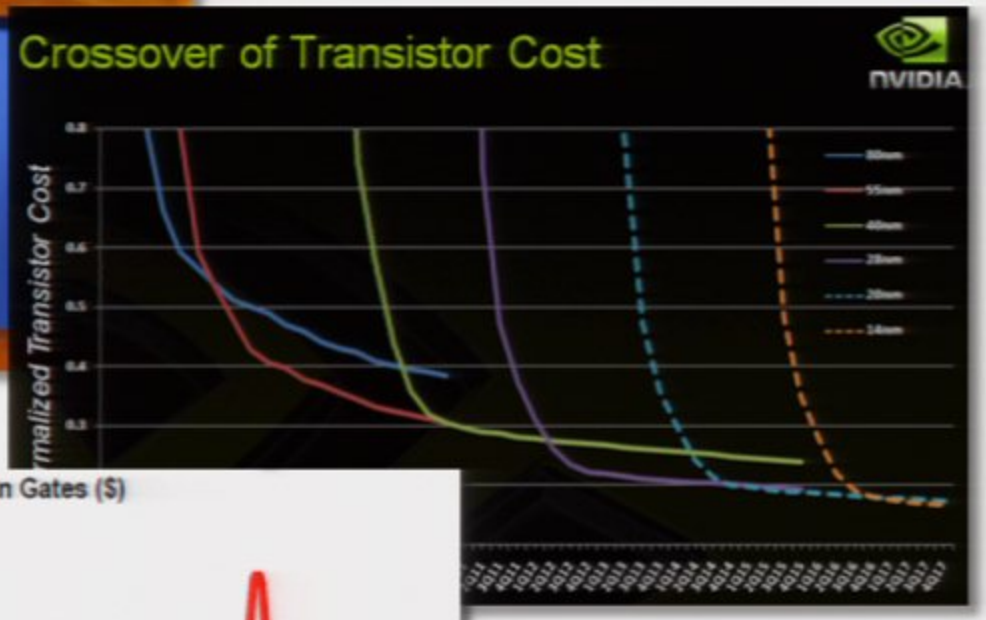


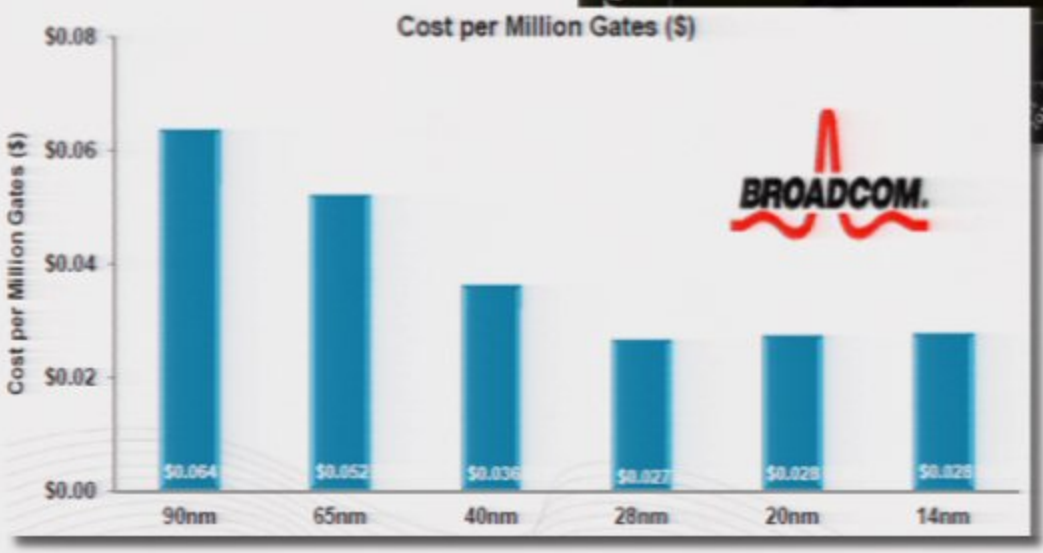


Sources: nVidia, ITPC, Nov, 2011
Broadcom, IMEC, May 2012
GF, ISS, Jan 2013

Cost becomes a concern post 28 nm







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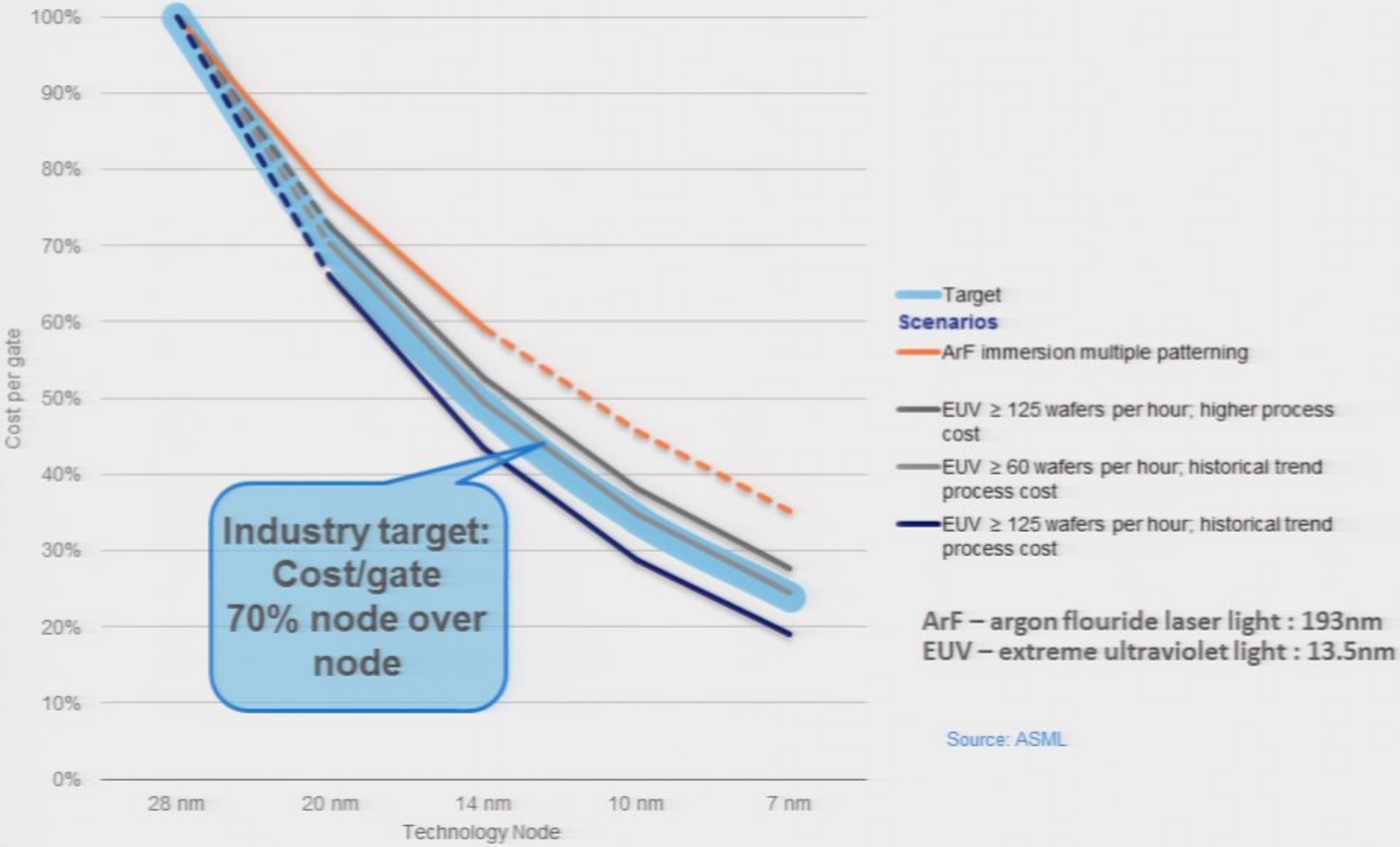
Litho roadmap supports cost per gate roadmap

EUV needed to enable industry target

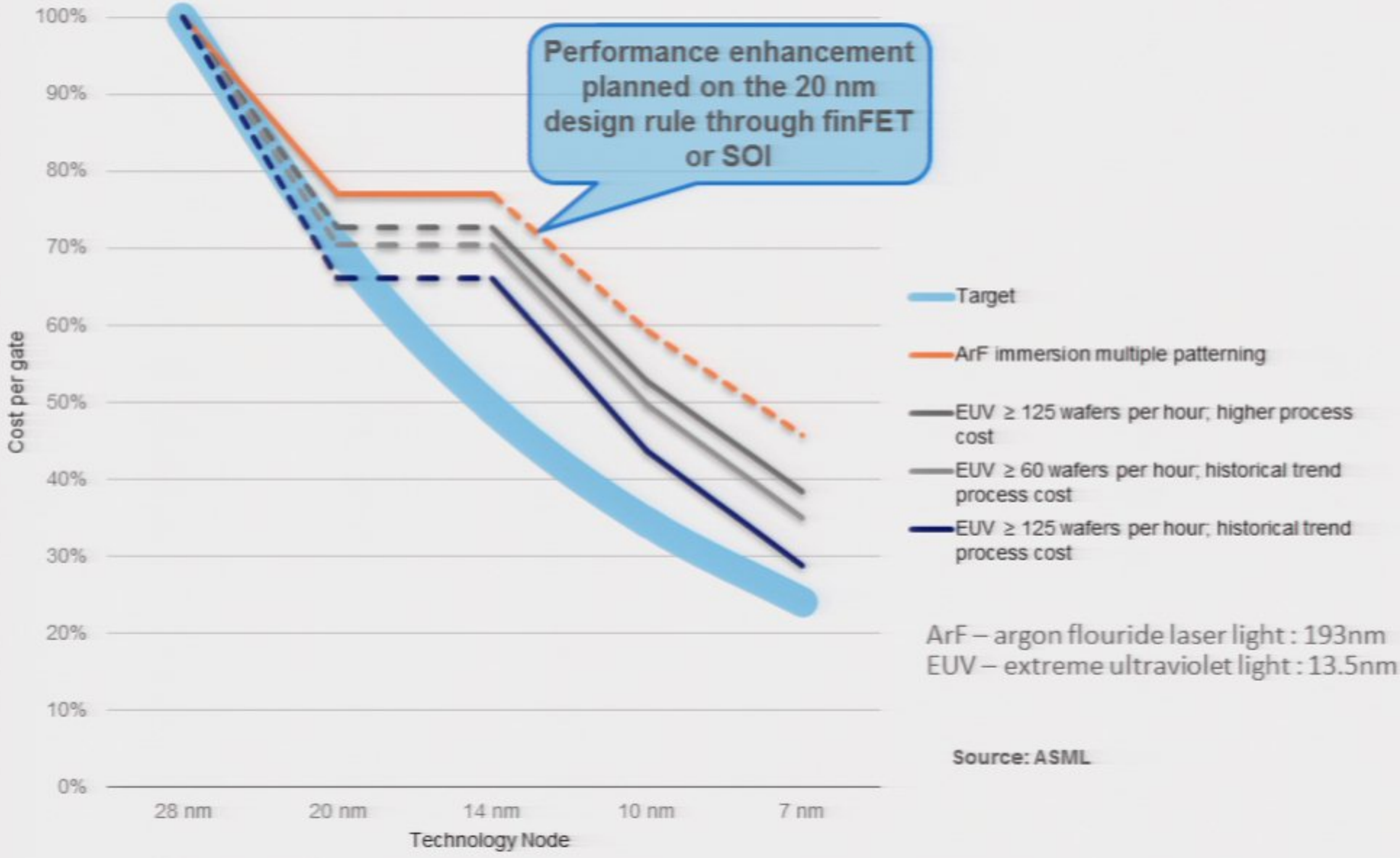


ArF – argon flouride laser light : 193nm
EUV – extreme ultraviolet light : 13.5nm

Source: ASML

Litho roadmap supports cost per gate roadmap

EUV needed to enable industry target



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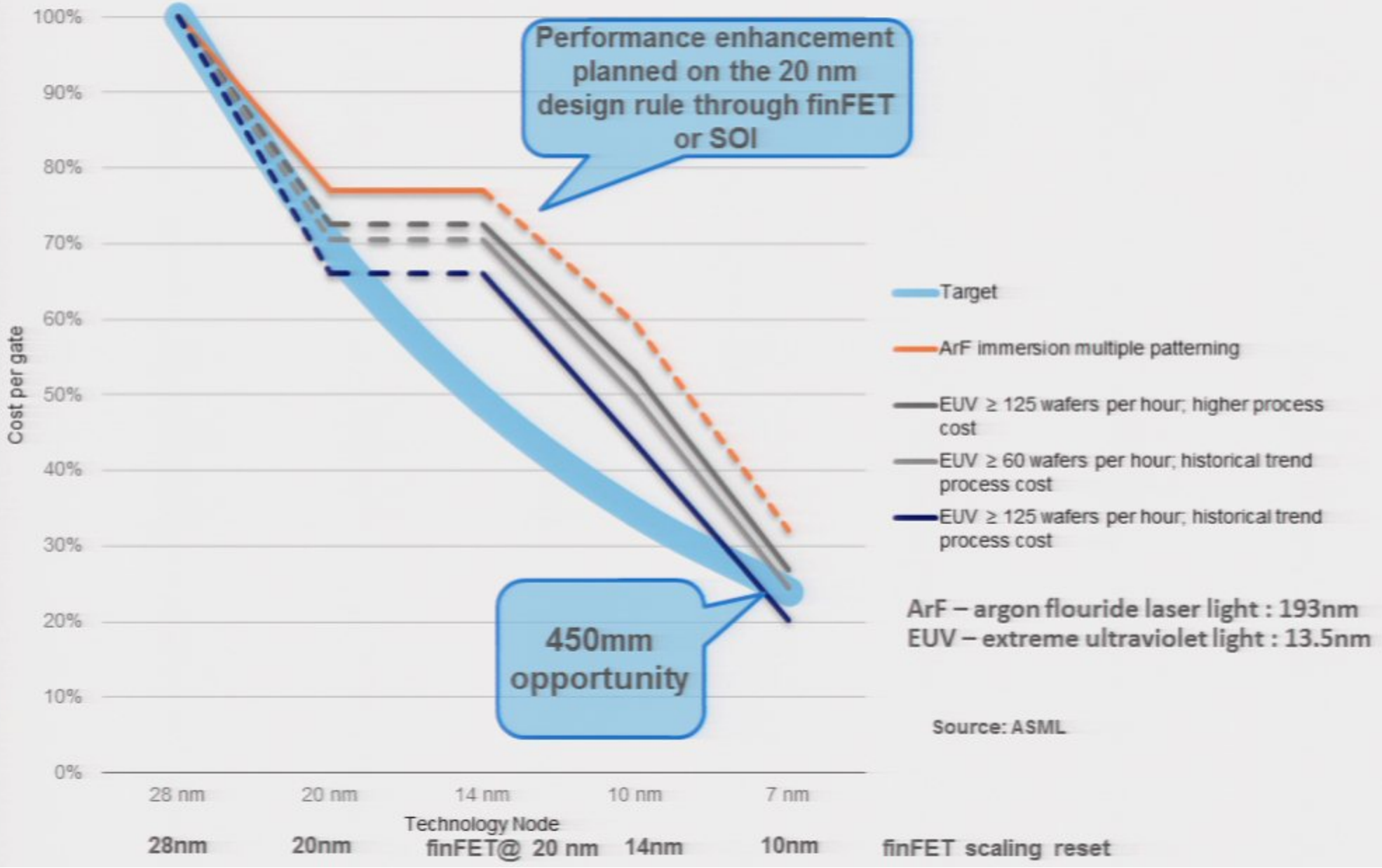


Affordable shrink roadmap

2012 2013 2014 2015 2016 2017 2018 2019 2020

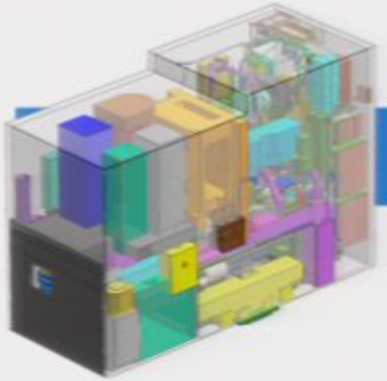
Immersion

NXT:1950i, NXT:1960Bi, NXT:1970Ci

EUV

NXE:3300B, NXE:3350, …

450mm



QXT, QXE

Affordable shrink roadmap

2012 2013 2014 2015 2016 2017 2018 2019 2020

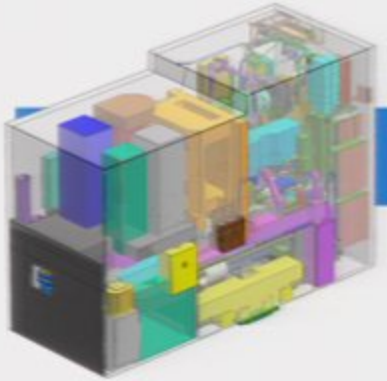
Immersion

Performance scaling on Immersion litho:
On Product Overlay (OPO) <8.5 nm → < 3 nm
Critical Dimension Uniformity (CDU) <2.0 nm → 1 nm
Throughput 200 wafers per hour (wph) → >250 wph

EUV

NXE:3300B, NXE:3350, …

450mm



QXT, QXE

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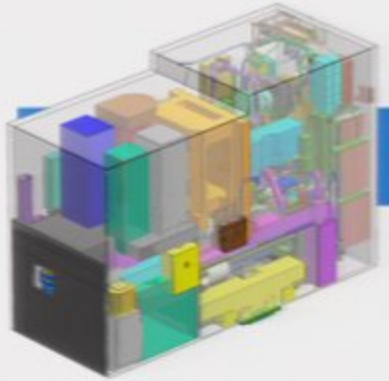
EUV

Economics and extendibility of EUV:
Resolution 22 nm → 8 nm
EUV to immersion overlay 5.0 nm → 2 nm
Throughput 70 wph → >125 wph

450mm



QXT, QXE

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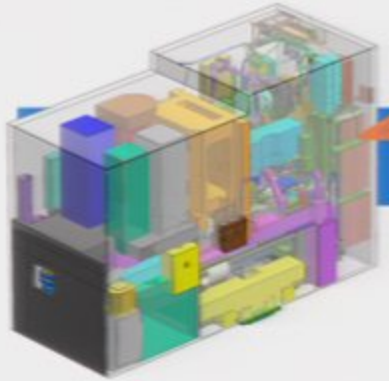


Cost opportunity of 450 mm:
Boost throughput measured in dies
No litho cost increase per die

Affordable shrink roadmap

2012 2013 2014 2015 2016 2017 2018 2019 2020

Immersion

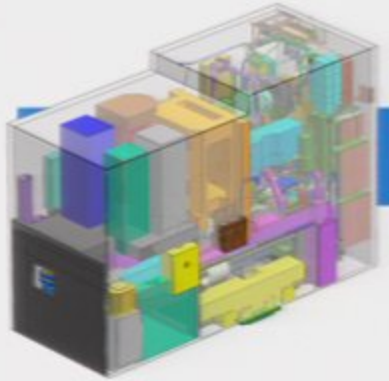
NXT:1950i, NXT:

EUV

N

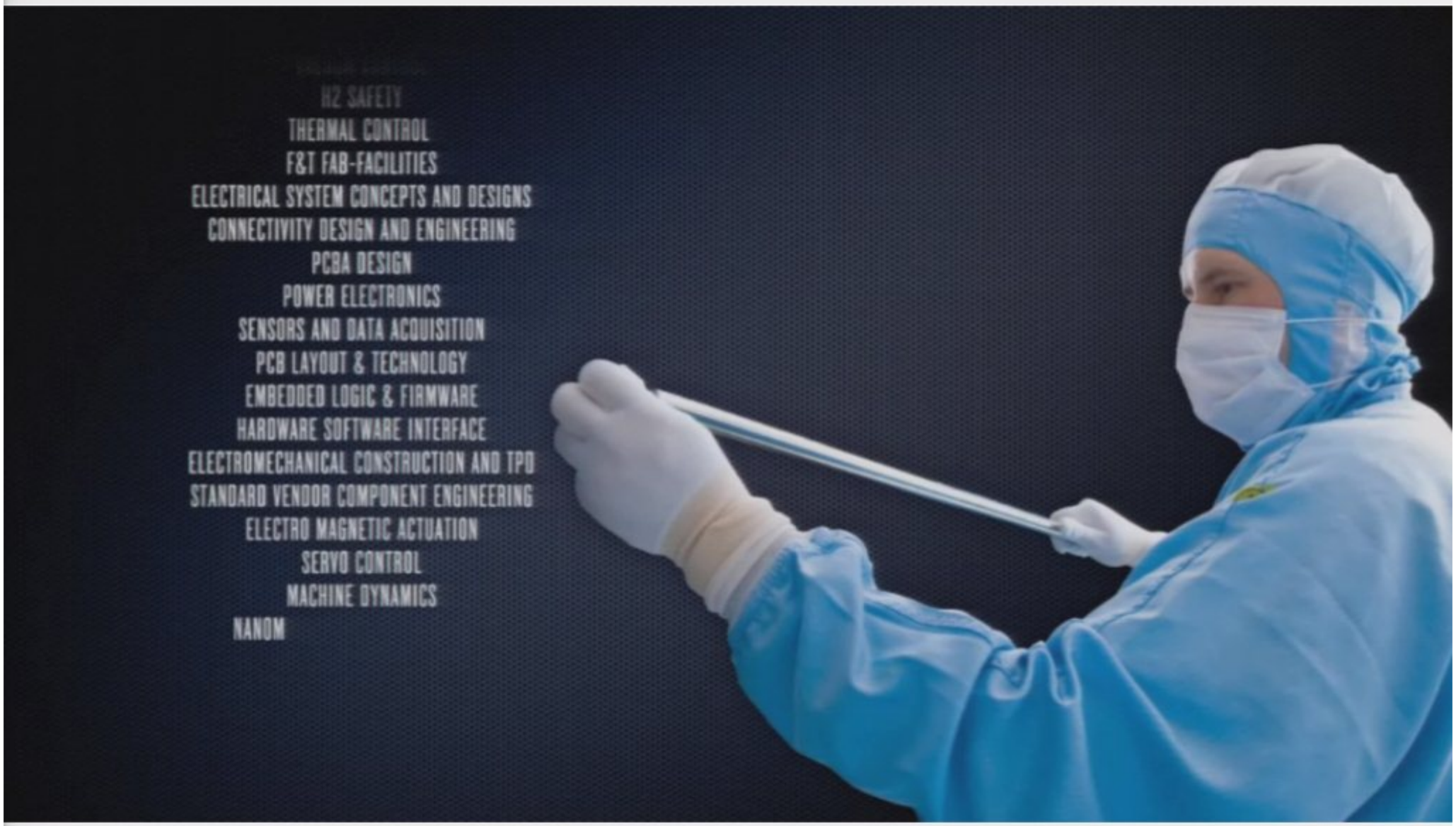
Supported by a Holistic Lithography approach using computational litho, overlay & CD metrology and feedback loops

450mm

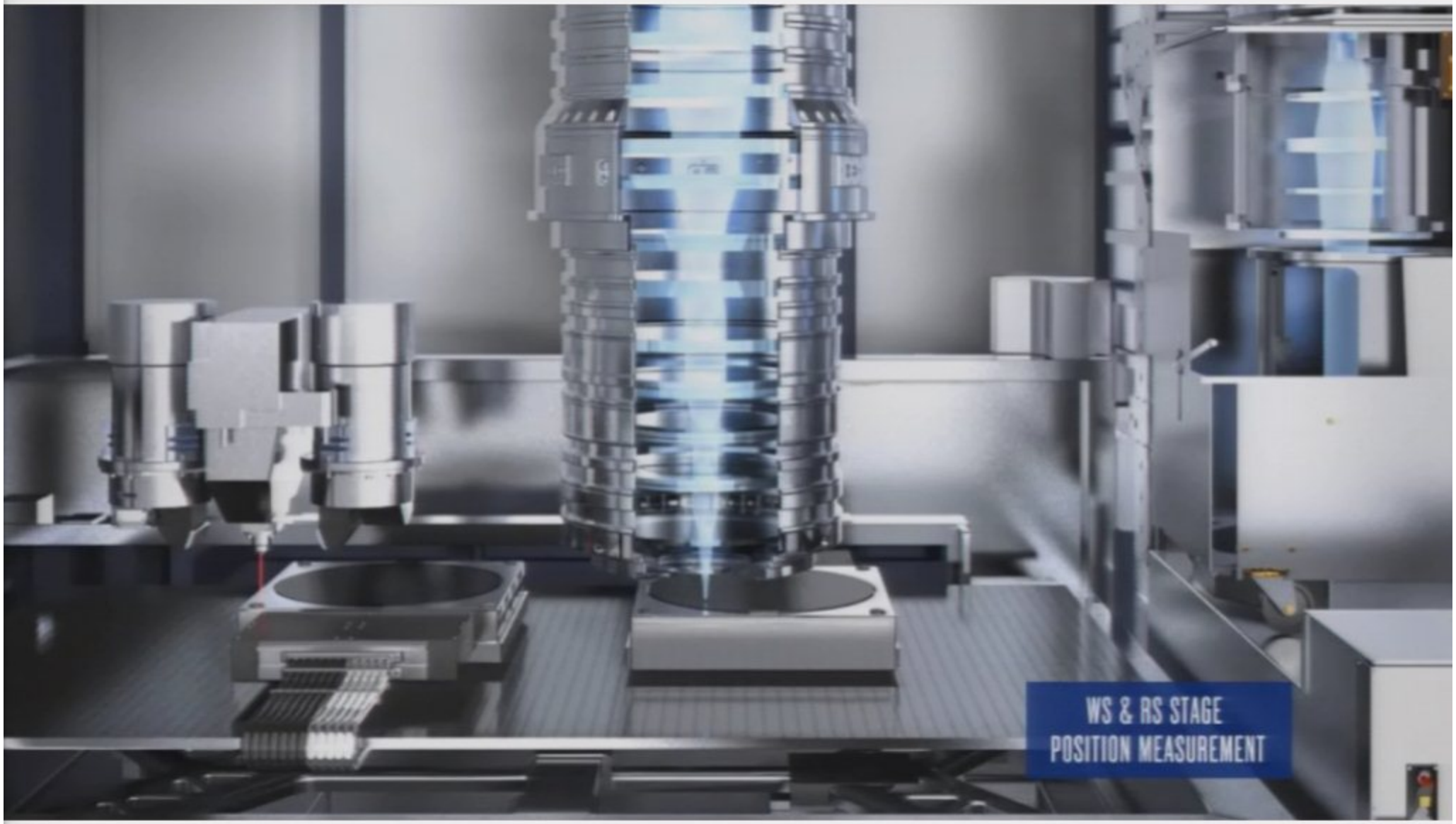


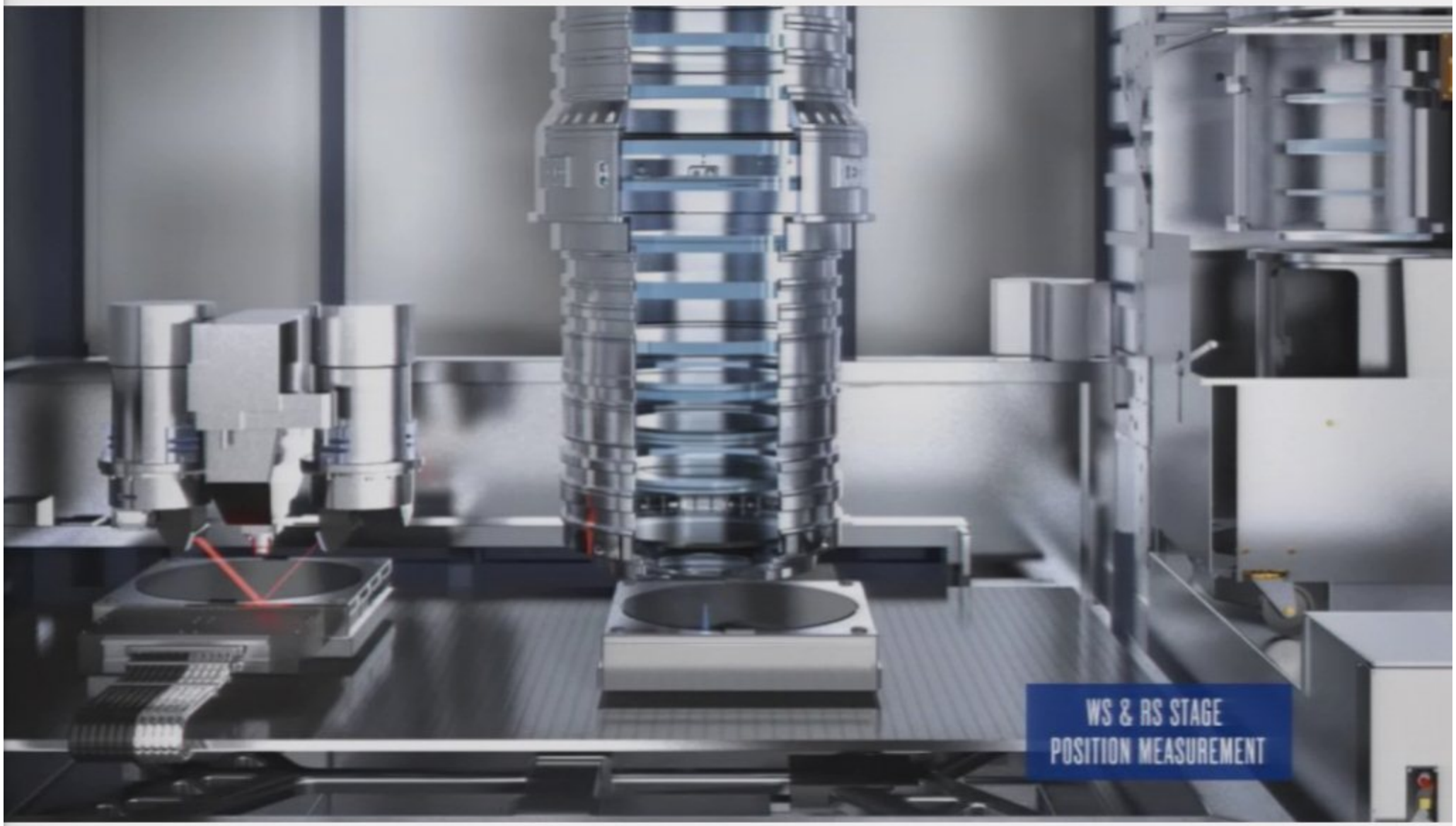
QXT, QXE

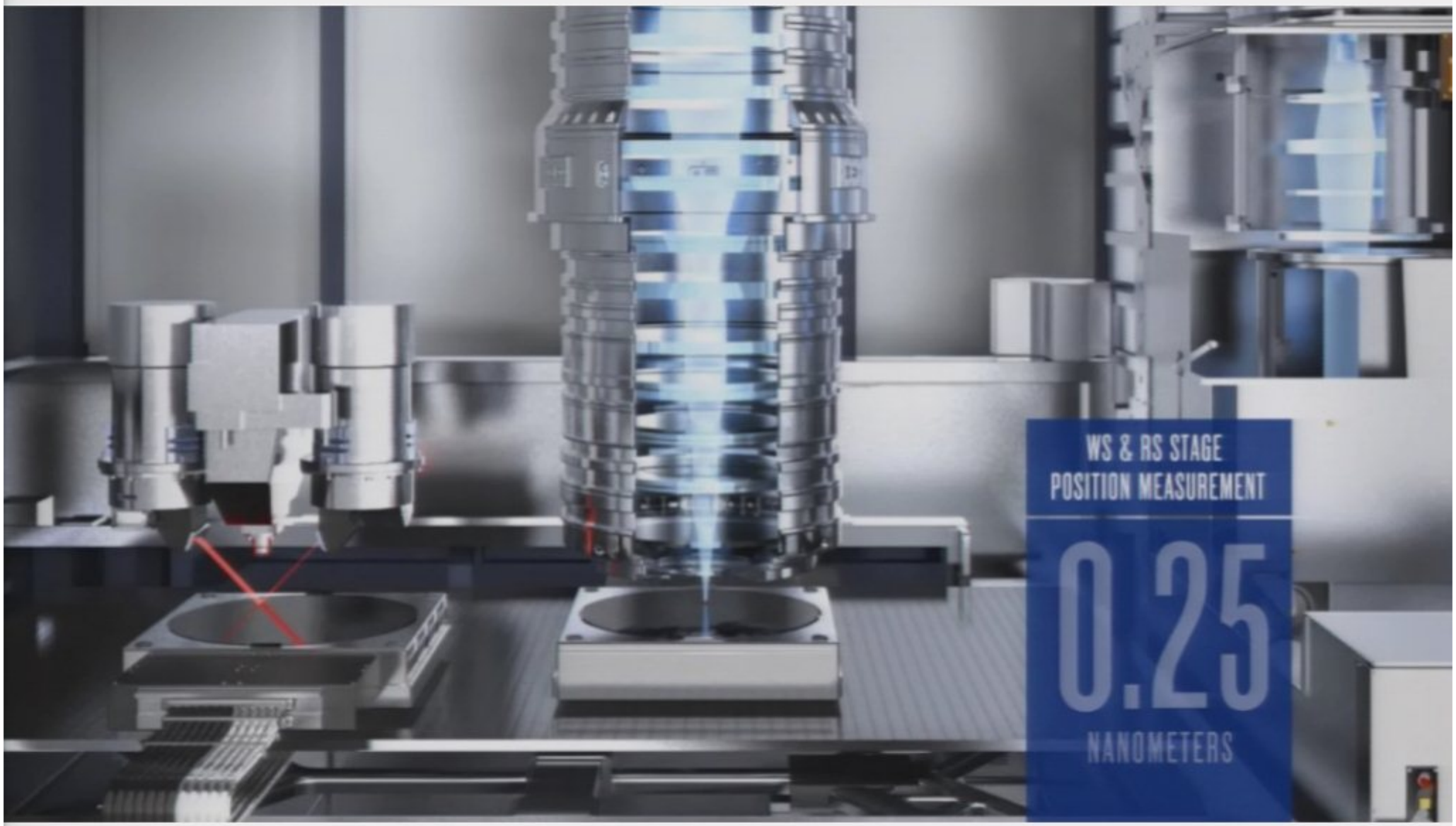

SOFTWARE
MECHANICAL ENGINEERING
MECHATRONICS
PHYSIC
ELECTRO
MATERIALS SCIENCE
MATHEMATICS

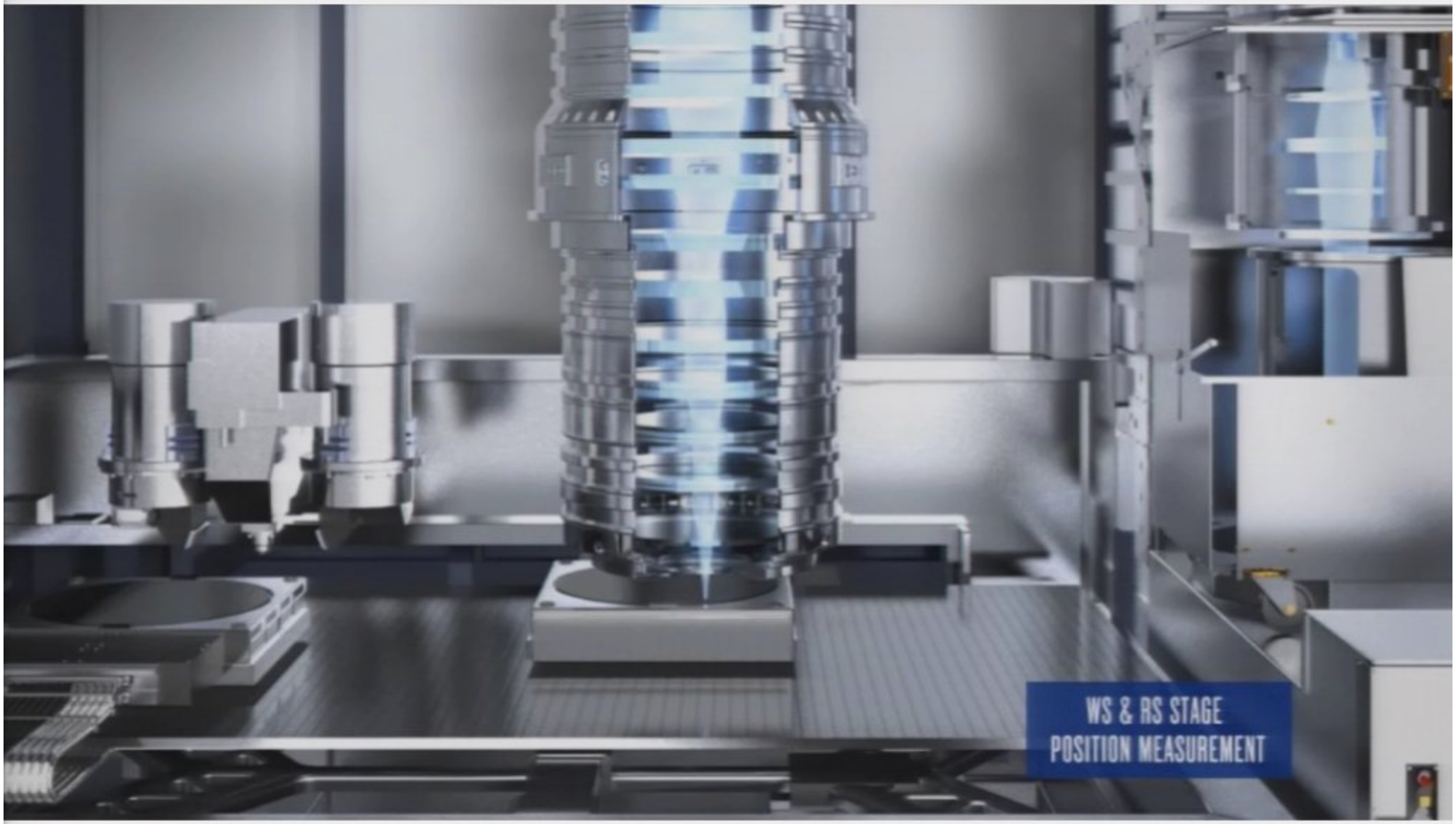

H2 SAFETY
THERMAL CONTROL
F&T FAB-FACILITIES
ELECTRICAL SYSTEM CONCEPTS AND DESIGNS
CONNECTIVITY DESIGN AND ENGINEERING
PCBA DESIGN
POWER ELECTRONICS
SENSORS AND DATA ACQUISITION
PCB LAYOUT & TECHNOLOGY
EMBEDDED LOGIC & FIRMWARE
HARDWARE SOFTWARE INTERFACE
ELECTROMECHANICAL CONSTRUCTION AND TPD
STANDARD VENDOR COMPONENT ENGINEERING
ELECTRO MAGNETIC ACTUATION
SERVO CONTROL
MACHINE DYNAMICS
NANOM


IMAGING
OVERLAY
FOCUS
PRODUCTIVITY
COST OF OWNERSHIP
COST OF GOODS
COST ADDED ASML
AVAILABILITY
CYCLE TIME
SAFETY
CONFIGURATIONS
SOFTWARE LAYOUT
SOFTWARE FACILITIES
MOTION CONTROL
COMPUTER SYSTEMS
DIAGNOSTIC FACILITIES
STAGE POWER CABINETS
ELECTRICAL S
MECHANICAL LAYOUT

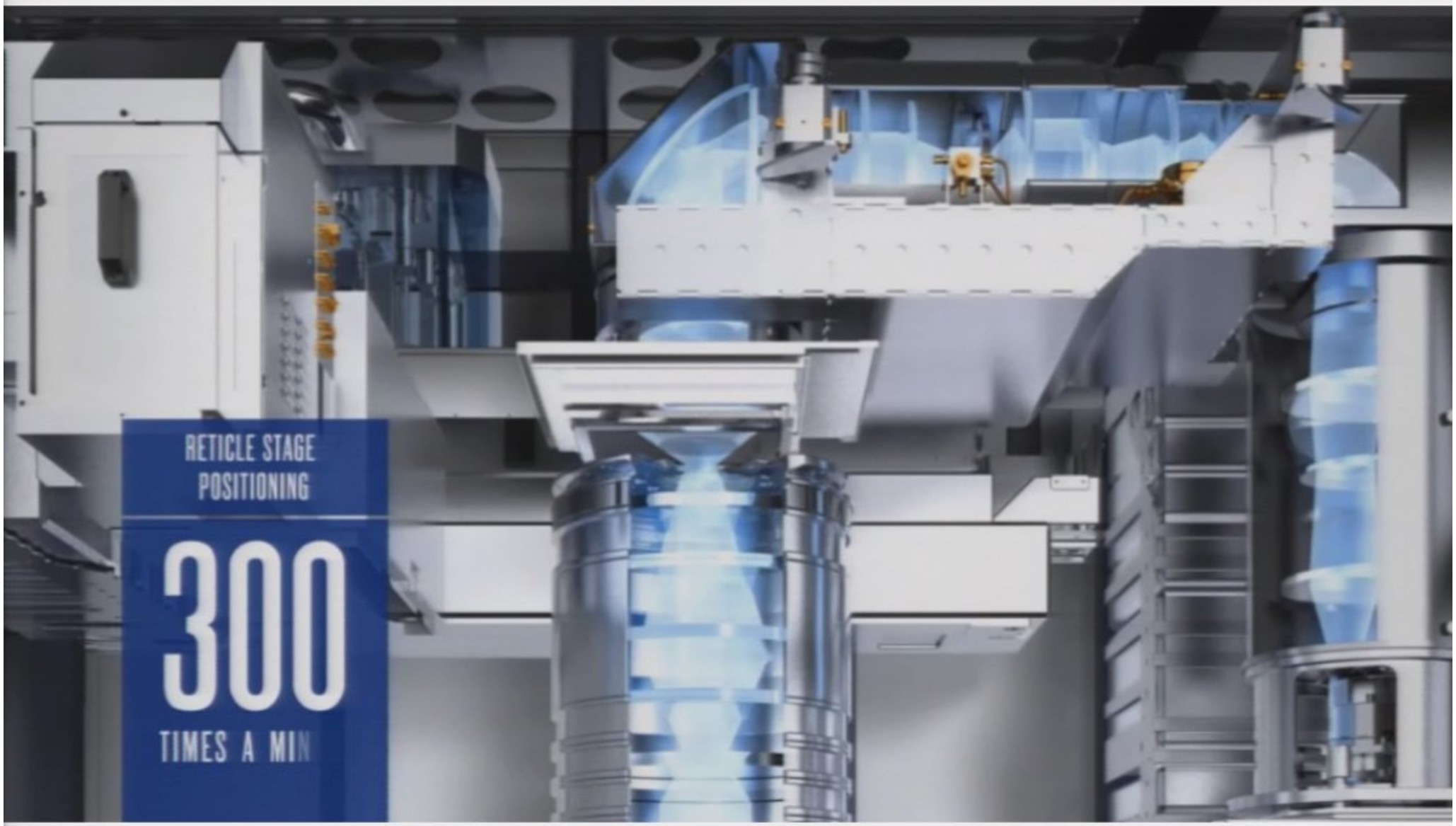

WS & RS STAGE
POSITION MEASUREMENT


WS & RS STAGE
POSITION MEASUREMENT


WS & RS STAGE
POSITION MEASUREMENT
0.25
NANOMETERS


WS & RS STAGE
POSITION MEASUREMENT


RETICLE STAGE
POSITIONING
13G


RETICLE STAGE
POSITIONING
300
TIMES A MIN


SYSTEM
SYNCHRONIZATION

SYSTEM
SYNCHRONIZATION

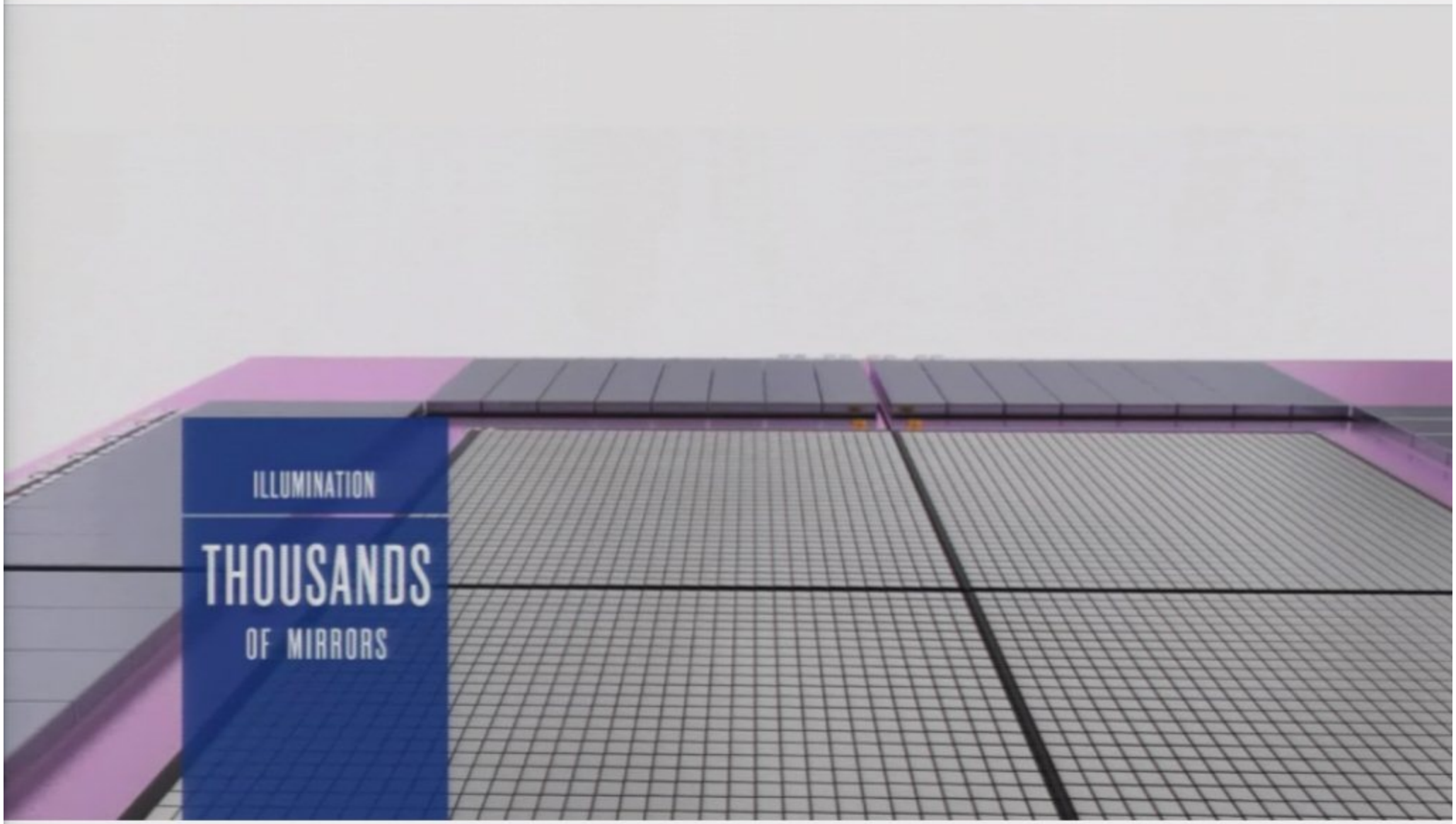
SYSTEM
SYNCHRONIZATION

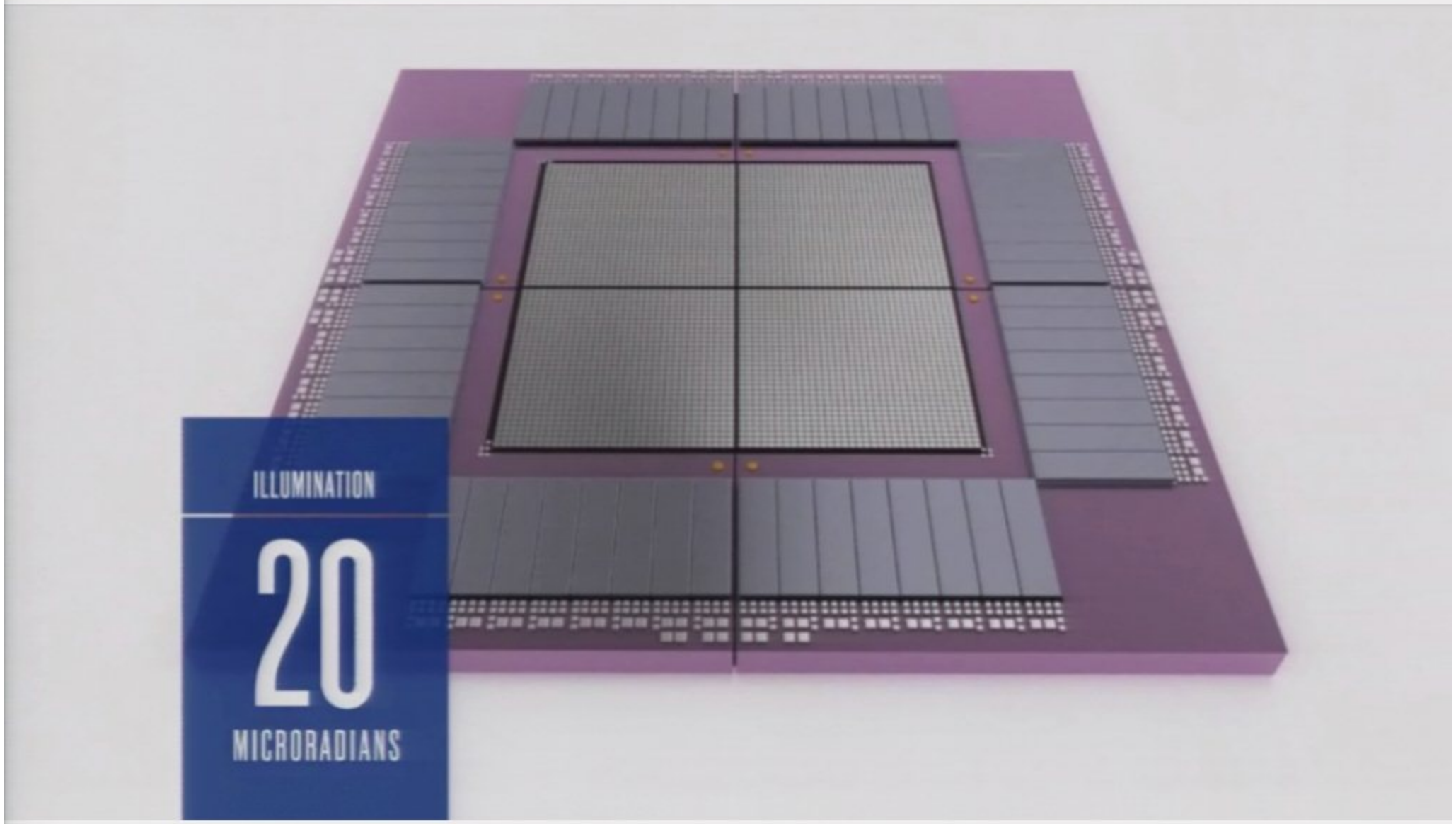
WITHIN

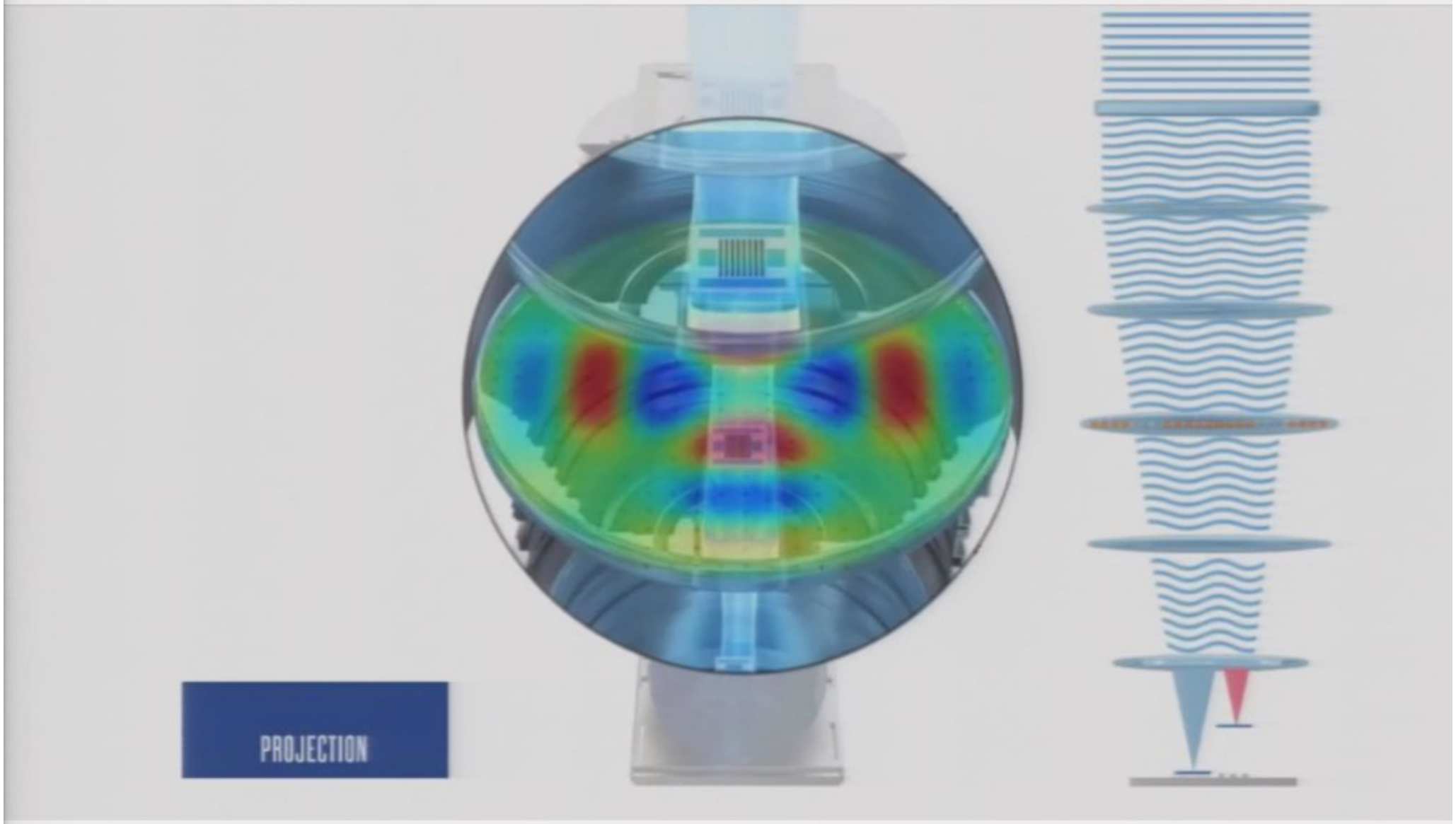
PICOSECONDS

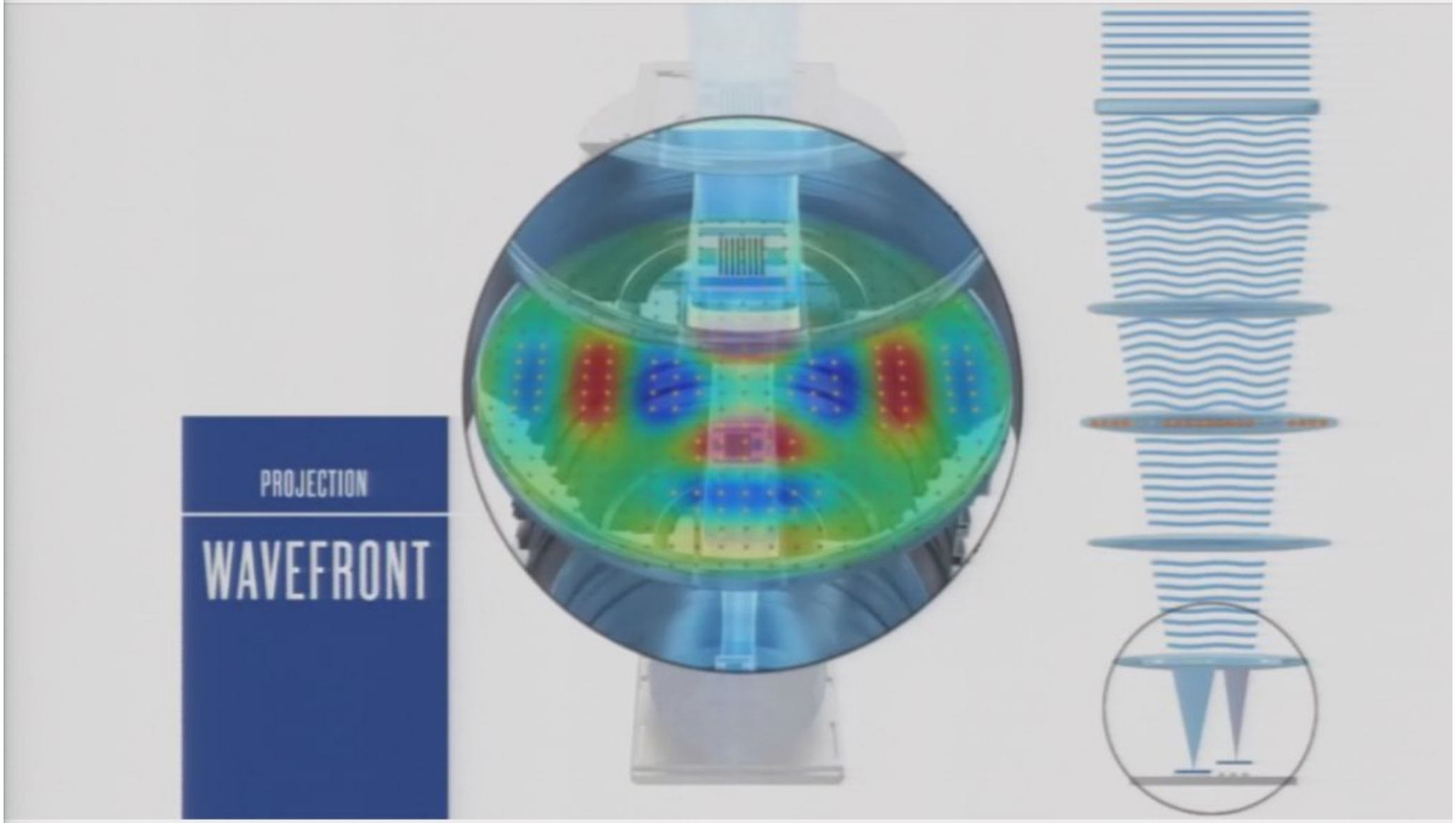

THERMAL
ARCHITECTURE

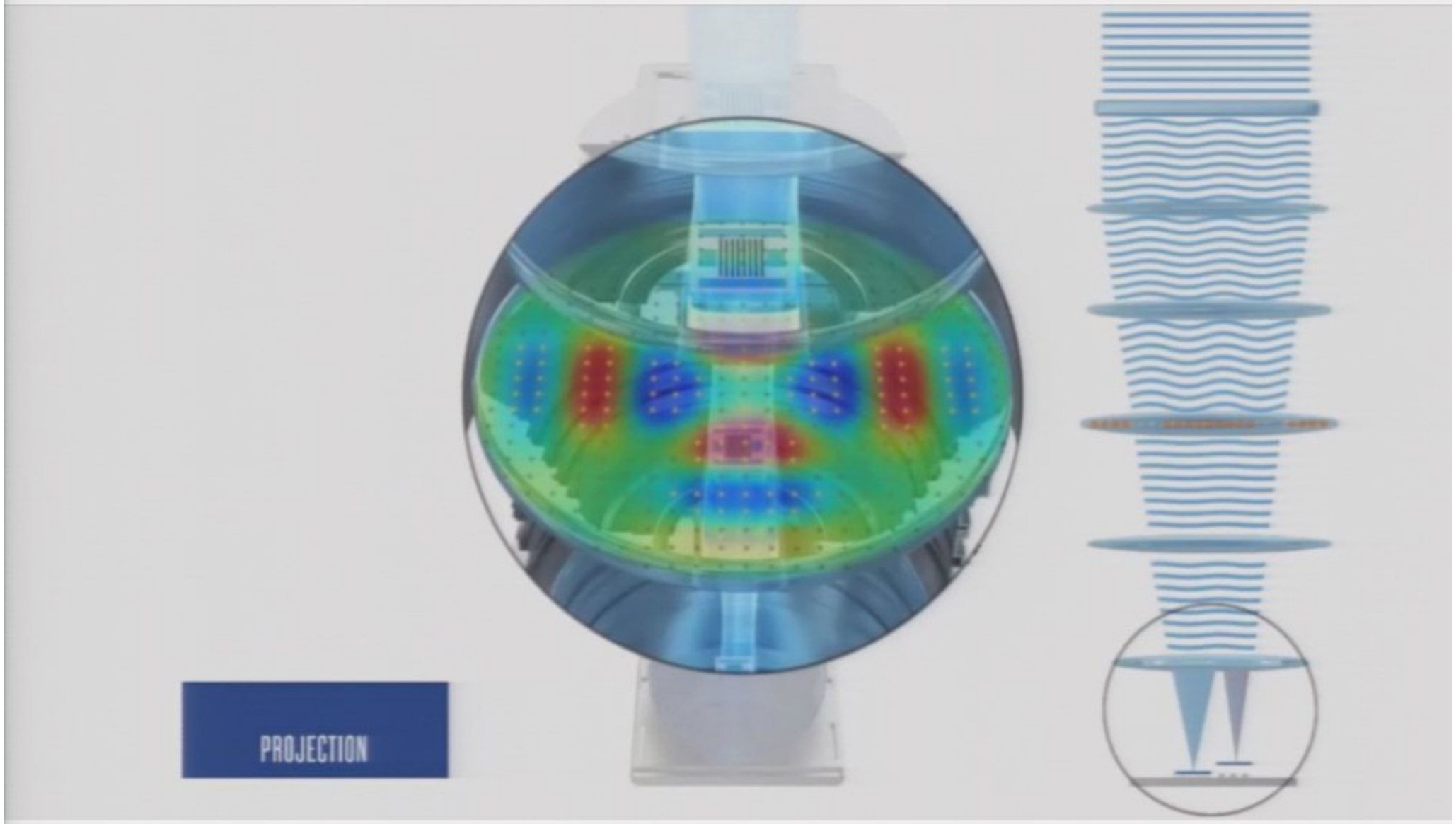

THERMAL
ARCHITECTURE


ILLUMINATION
THOUSANDS
OF MIRRORS

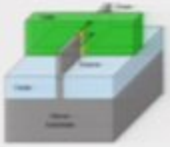
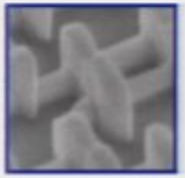
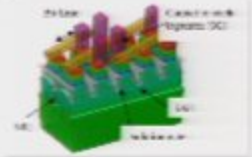
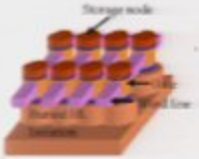
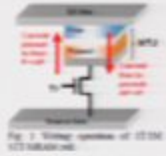
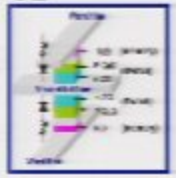

ILLUMINATION
20
MICRORADIANS


PROJECTION


PROJECTION
WAVEFRONT


PROJECTION

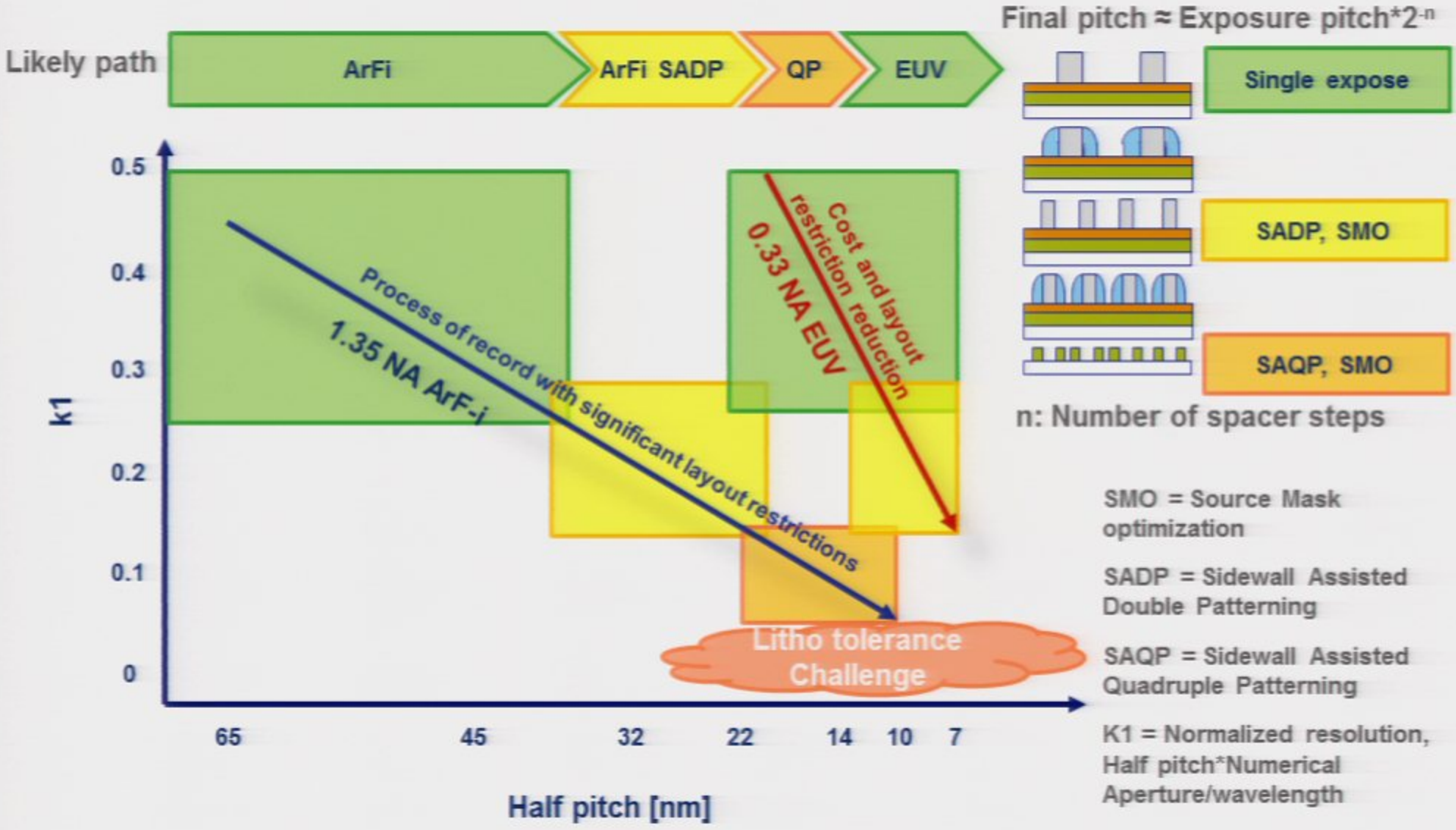
IC manufacturers' roadmaps supports further scaling

	2012 - 2013	2014 - 2015	2016 - 2017	2018 - 2019
Logic	**22 - 20 nm node** **Memory:** 0.09um2, SRAM **Device:** planar or FinFET (Intel) **Gate:** RMG-HKMG **Channel:** Si **Vdd:** 0.8V 	**16 - 14 nm node** **Memory:** 0.08um2 SRAM **Device:** FinFET, FDSOI **Gate:** RMG-HKMG **Channel:** Si; (Si)Ge **Vdd:** 0.6V 	**11 - 10 nm node** **Memory:** 0.06um2 SRAM **Device:** FinFET **Gate:** HKMG **Channel:** Si, Ge, IIIVr **Vdd:** 0.5V 	**8 - 7 nm node** **Memory:** FBRAM, STT-RAM, >8TSRAM **Device: FinFET,** Nanowire, TFET **Gate:** HKMG **Channel:** IIIV-Graphene 
DRAM	**38 - 32 nm node** **Memory:** stacked MIM **Peri:** planar **Array:** 6F2, bWL **Gate:** poly/SiO2 **Channel:** Si **Vdd**=1.35V 	**29 - 22 nm node** **Memory:** stacked MIM **Peri:** planar HKMG **Array:** 6F2, bWL **Gate:** HKMG **Channel:** Si **Vdd**=1.2V 	**22 - 16 nm node** **Memory:** stacked MIM **Peri:** planar **Array: 6F2,** 4F2, bBL, LBL, 1T1C(VFET) **Gate:** HKMG **Channel:** Si **Vdd**=1.1V 	**16 - 14 nm node** **Memory:** FBRAM, STT-MRAM, RRAM, PcRAM **Peri:** planar **Array:** 4F2, 1T, 1T1R, 1T1MTJ(VFET) **Gate:** HKMG **Channel:** Si **Vdd**~1V 
Flash	**19 - 16 nm hp** **4.5F - 6F2 asymm. cell** **Density:** 128G **Device:** FG 	**16 - 13 nm hp** **3D NAND intro at 5x → 4x nm** **6F2 asymmetric cell** **4F2 symmetric cell** **Density:** 256-512G **Device:** dual-FG 	**~ 11 nm hp (planar)** **3D NAND at 3x → 2x nm** **X-pt intro at 2x nm** **7F2 asymmetric cell** **4F2 symmetric cell** **Density:** 512-1024G **Device::** dual-FG, BiCS in HVM(@4xnm)	**< 10 nm hp (planar)** **X-pt intro at 2x nm** **Density:** > 1T with 3D chip stacking **Device:** 3D BiCS, XPoint-RRAM **Selector:** diode 

Source: IMEC, ASML TDC, jan 2013

Cost-efficient 1D scaling with immersion to 10 nm half pitch

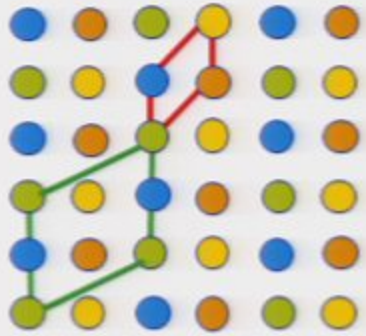
Applicable for NAND and µProcessor design



2D structures for Logic and DRAM scaling challenging

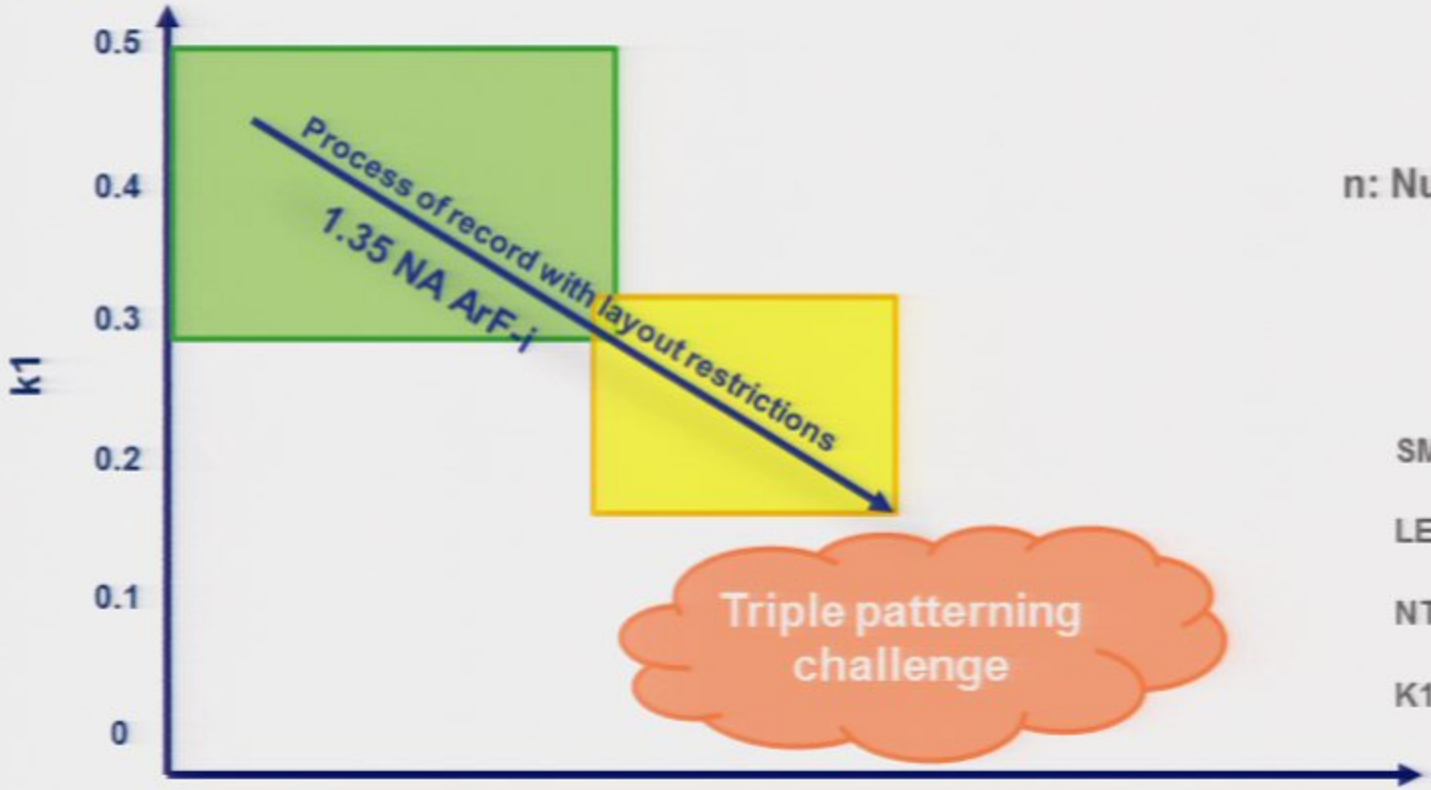
using double patterning on ArF immersion

Final pitch ≈ exposure pitch/√n



n: Number of exposures&etch

Likely path



Single expose

LELE, SMO,(NTD)

SMO = Source Mask optimization

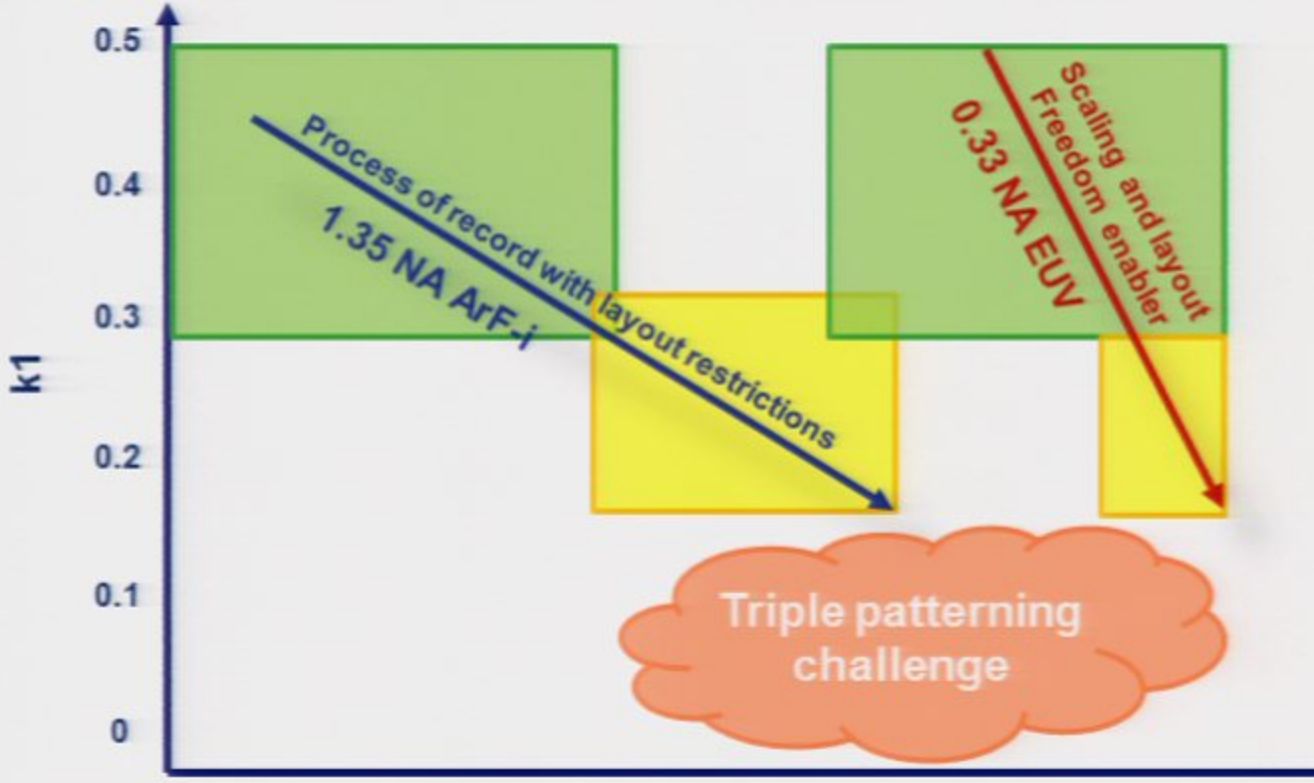
LELE = Litho Etch Litho Etch

NTD = Negative Tone Developer

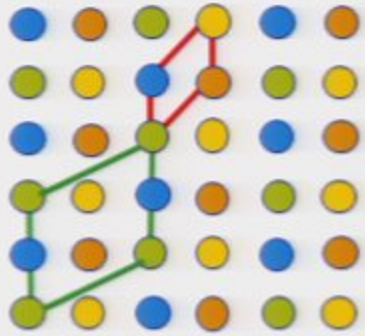
K1 = Normalized resolution, Half pitch*Numerical Aperture/wavelength

Therefore, EUV is needed for scaling down to 7 nm half pitch

Likely path: ArFi → ArFi LELE → EUV



Final pitch ≈ exposure pitch/√n



n: Number of exposures&etch

Single expose

LELE, SMO,(NTD)

SMO = Source Mask optimization

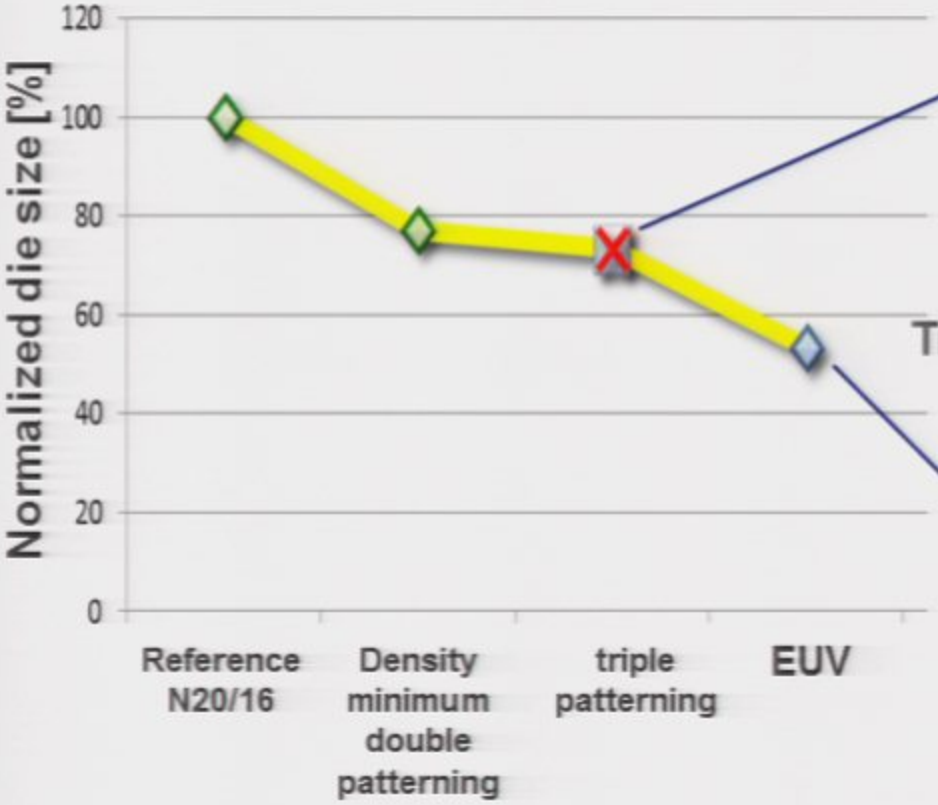
LELE = Litho Etch Litho Etch

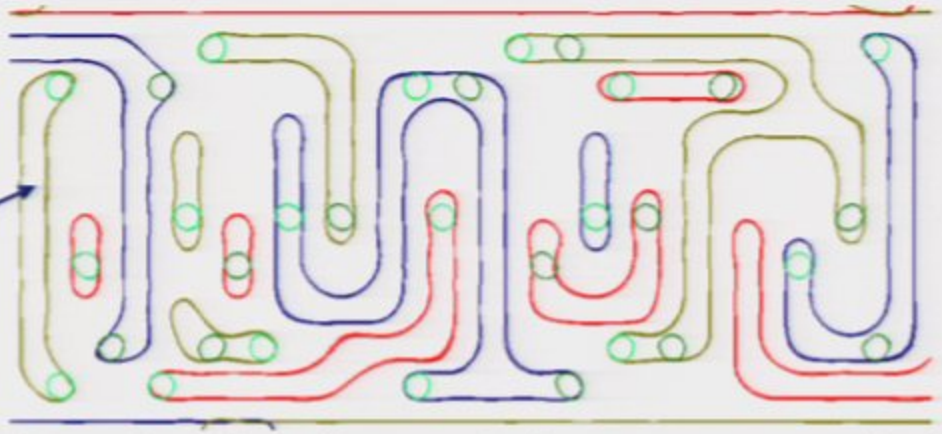
NTD = Negative Tone Developer

K1 = Normalized resolution, Half pitch*Numerical Aperture/wavelength

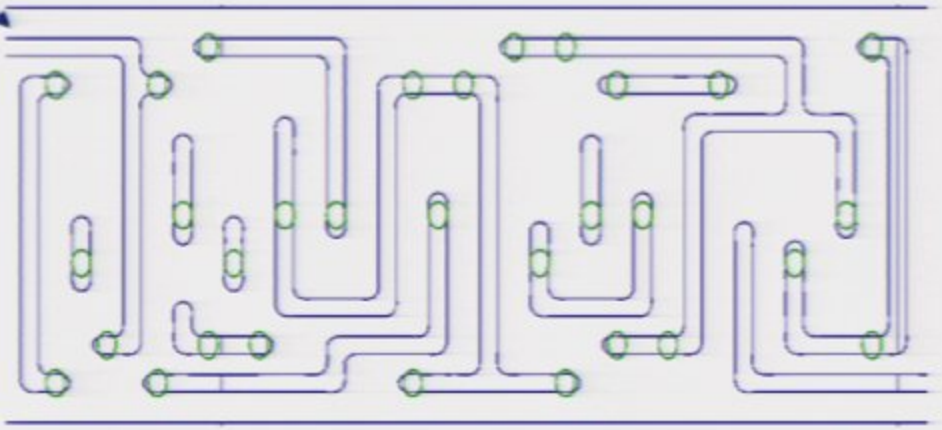
Logic: 50% scaling for 10 nm node only with EUV

Shrink limited to ~25% using immersion due to layout restrictions and litho performance





Triple patterning does not show process window

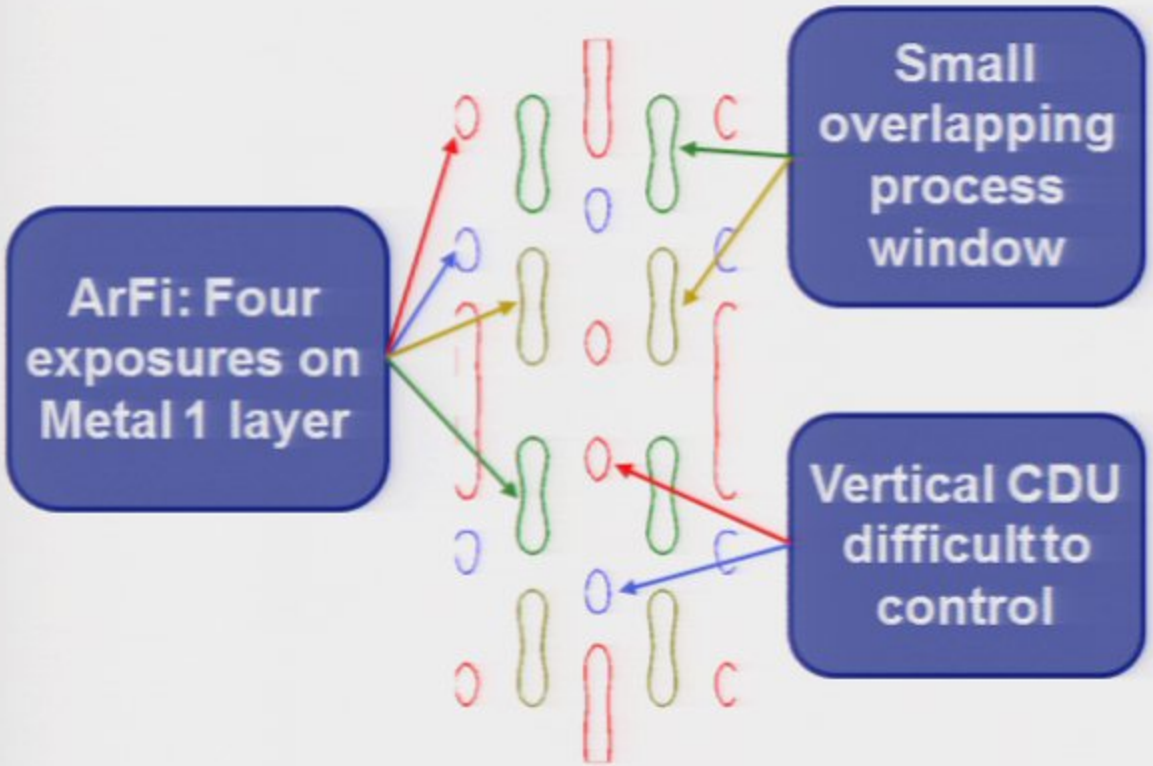


EUV meets all litho requirements

Source: ARM, Scaled N20 nm flip-flop design

Even gridded SRAM designs prefer EUV at 10 nm node

Critical overlay between local interconnect layers and CD variability make multiple patterning very difficult



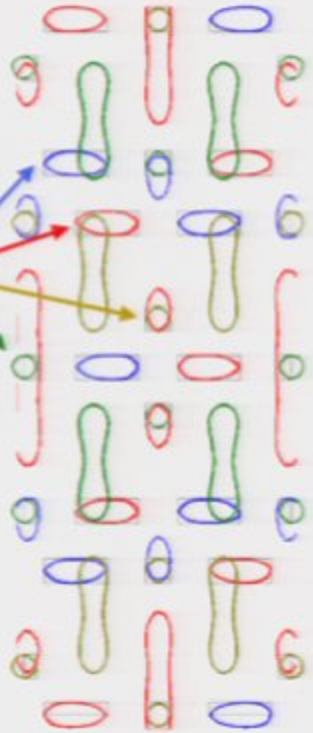
CDU – critical dimension uniformity

Source: ASML, Local interconnect layers for generic SRAM cell

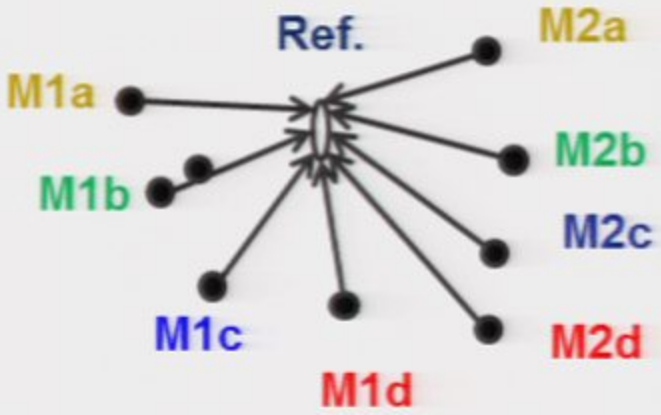
Even gridded SRAM designs prefer EUV at 10 nm node

Critical overlay between local interconnect layers and CD variability make multiple patterning very difficult

ArFi: Four exposures on Metal 2 layer



All exposures have to match to enable sufficient Metal 1 to 2 overlap, strongly tightening overlay requirements

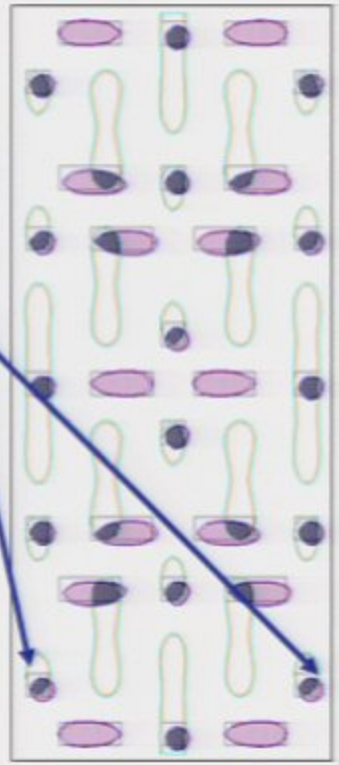


Source: ASML, Local interconnect layers for generic SRAM cell

Even gridded SRAM designs prefer EUV at 10 nm node

Critical overlay between local interconnect layers and CD variability make multiple patterning very difficult

ArFi Overlapping areas fail to meet spec even with 3 nm overlay



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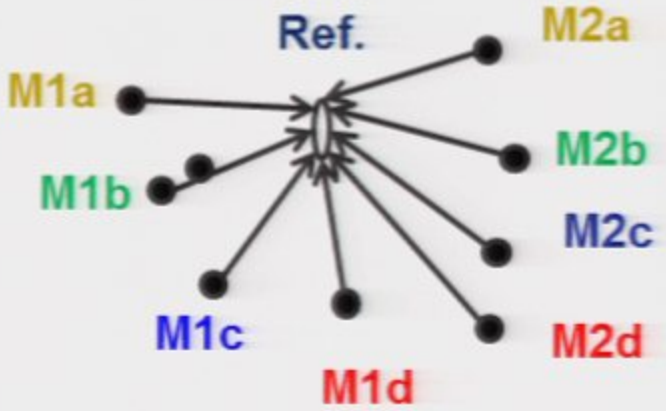
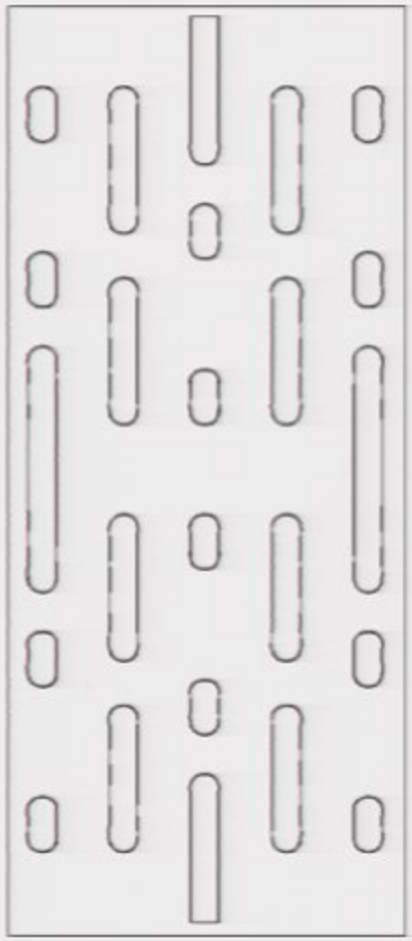


Source: ASML, Local interconnect layers for generic SRAM cell

Even gridded SRAM designs prefer EUV at 10 nm node

Critical overlay between local interconnect layers makes multiple patterning very difficult

EUV: Two single exposures



CD – critical dimension

Source: ASML, Local interconnect layers for generic SRAM cell

Even gridded SRAM designs prefer EUV at 10 nm node

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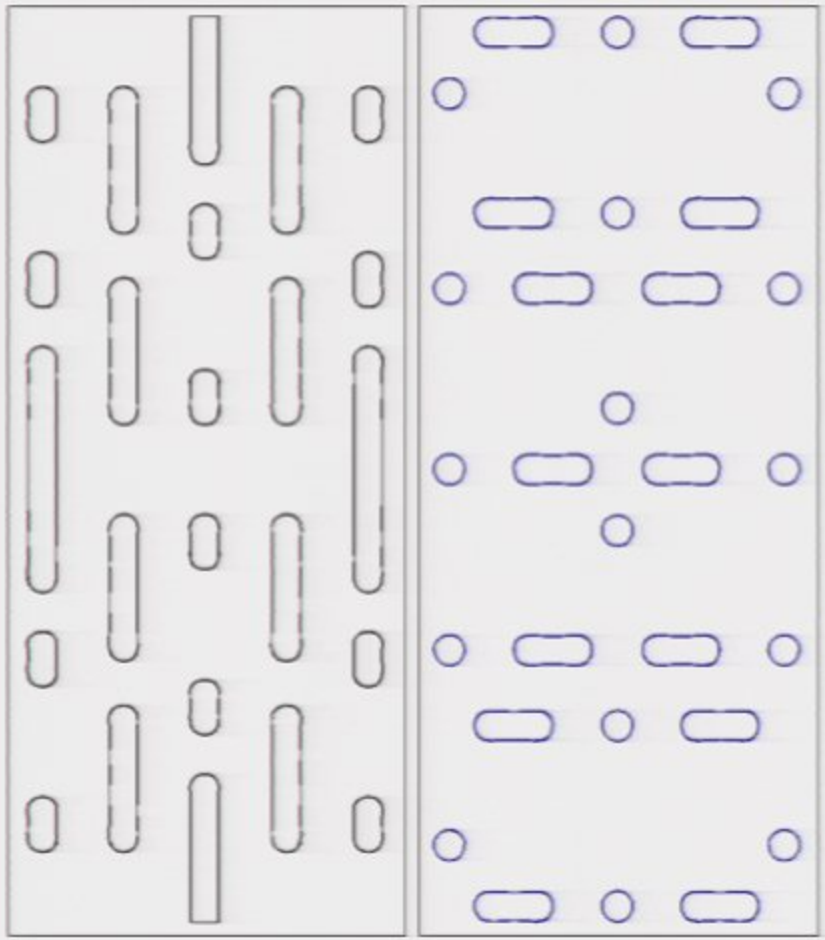

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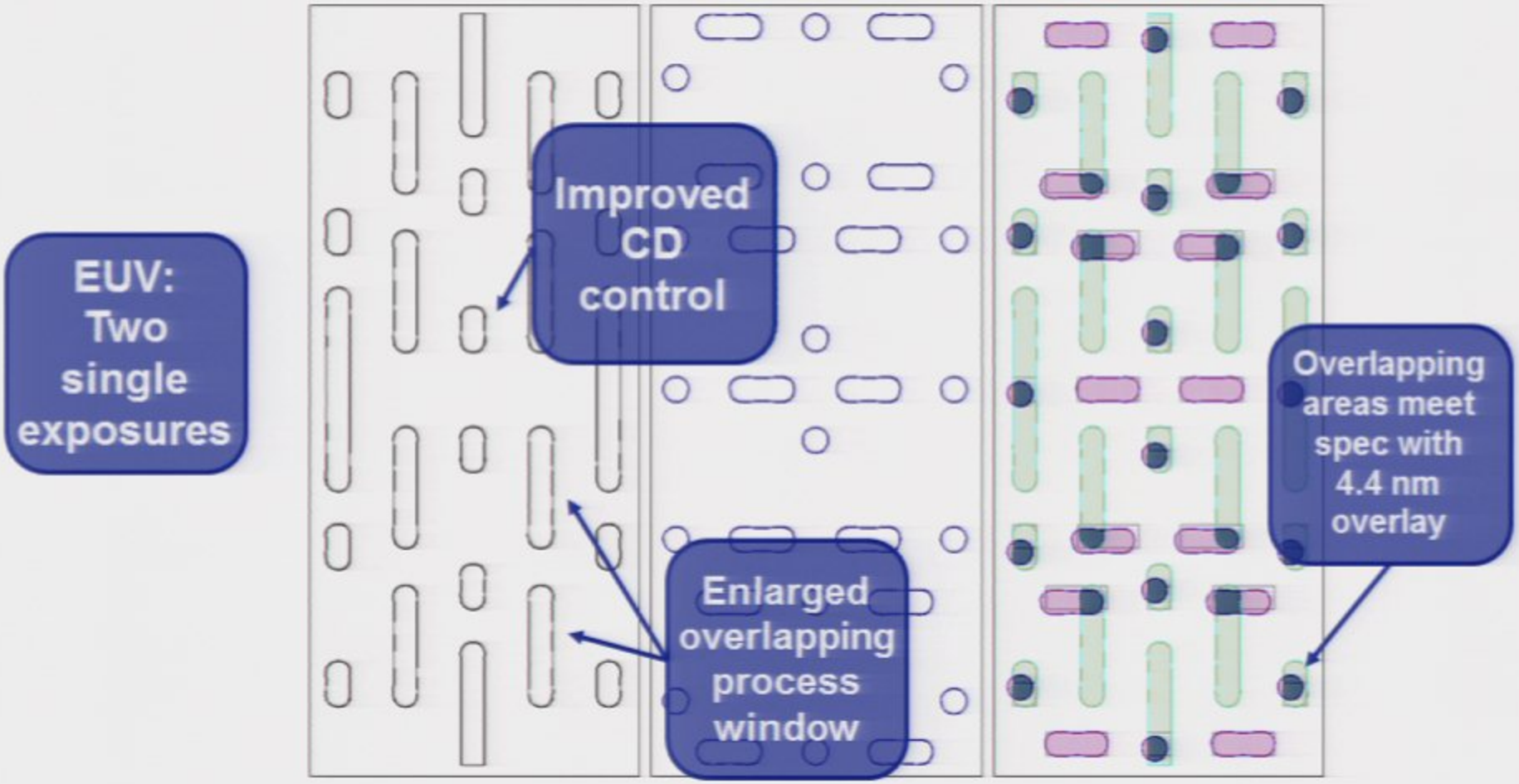


CD – critical dimension

Source: ASML, Local interconnect layers for generic SRAM cell

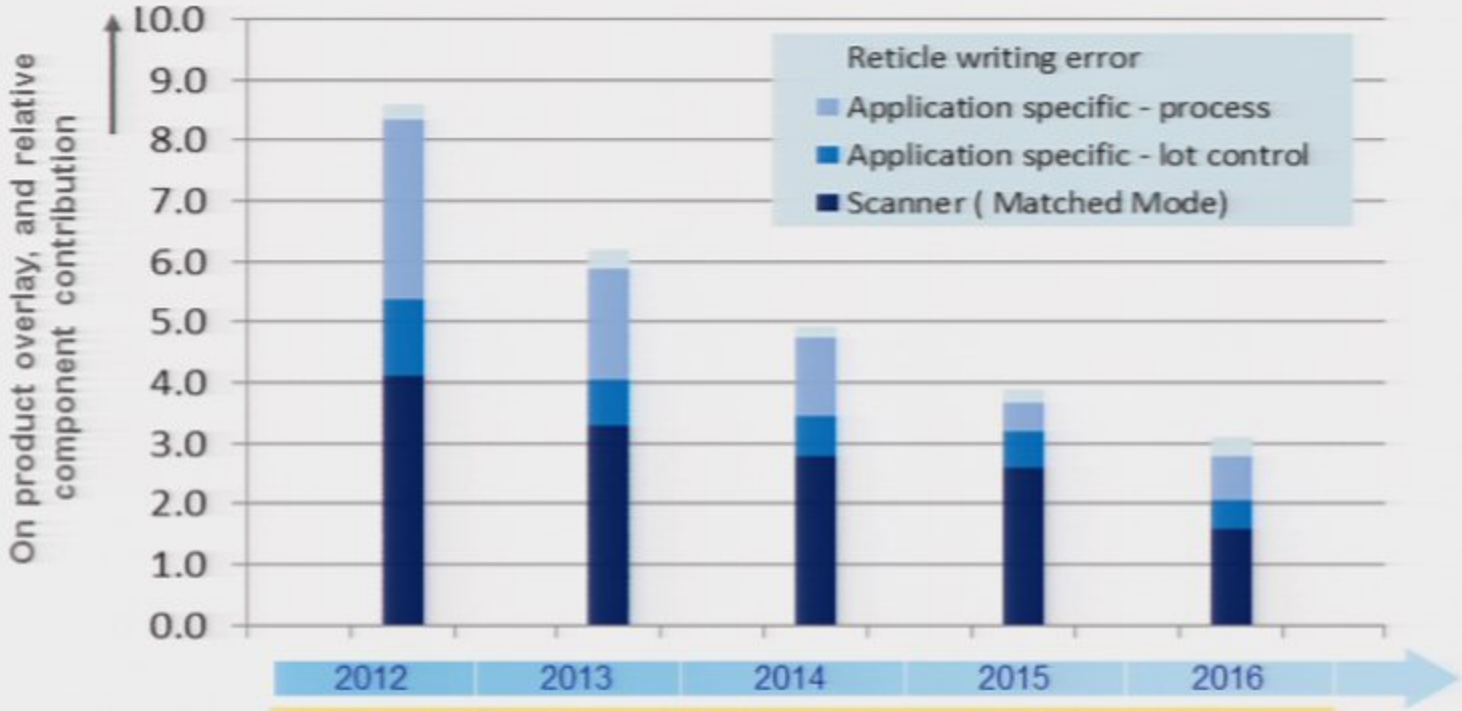
Shrink roadmap – summary

- The appetite for shrinking devices continues to be strong and will be technically feasible to well below 10 nm. The economics of scaling is an increasing issue.
- Current IC performance and power challenges fuel the fast introduction of high performance FinFETs at most foundries, called the 14 nm node on a 20 nm backend density.
- Double patterning using immersion is the current lithography shrink technology, however shrinking with this technology below the 20-14 nm density is only feasible when:
  - Design layouts are aligned on an single grid
  - Litho performance supports the multi patterning error budgets
  - Multiple patterning affordability is secured through high productivity and process simplicity
- EUV, over time supported by 450 mm, continues to be the only affordable shrinking technology allowing desired increased layout flexibility for logic.

Agenda

- Shrink roadmap
- **Holistic Lithography on immersion platform**
- EUV lithography
- 450 mm
- Future

Holistic approach required to reduce overlay



On product overlay in matched machine mode – ASML Roadmap

8.5 nm	6 nm	5 nm	4 nm	3 nm

On product overlay contributors and roadmap

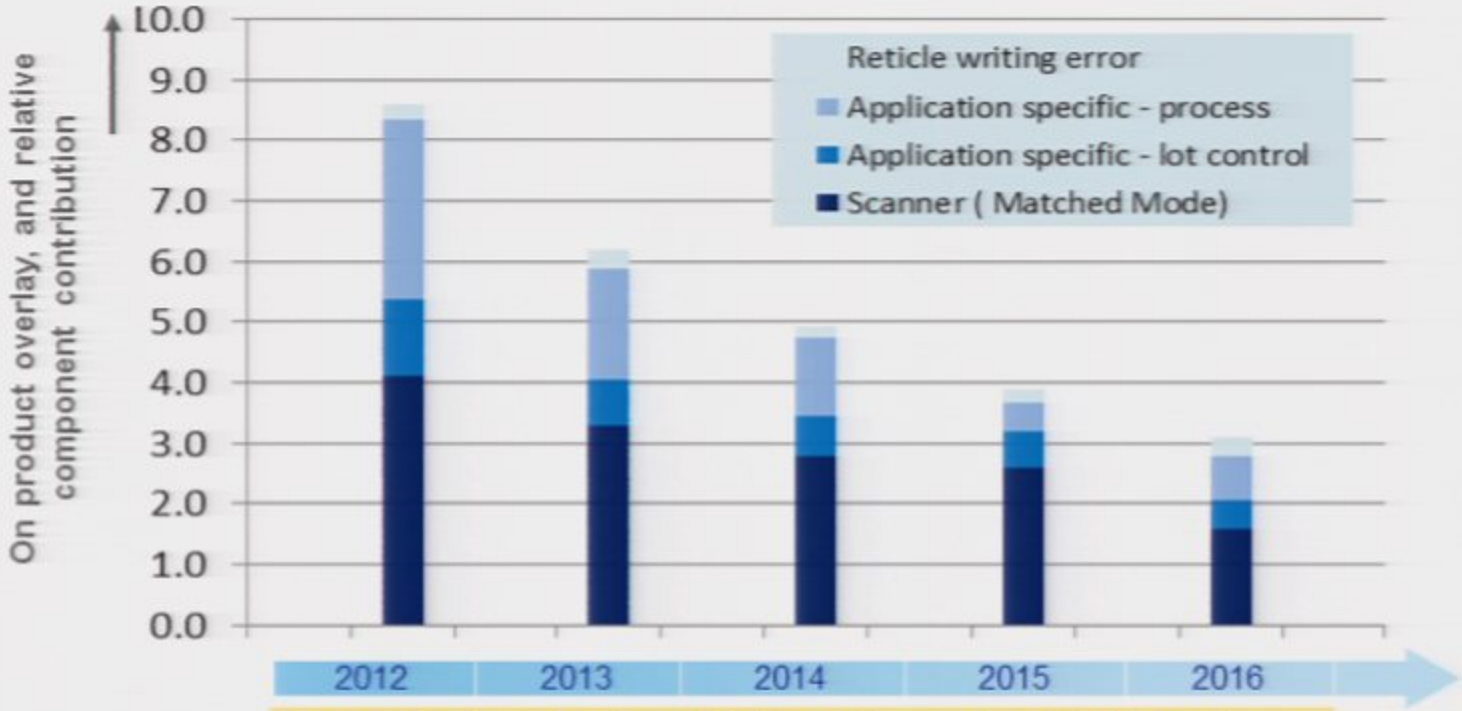
Notes:

On product overlay $=\sqrt{A^2 + B^2 + C^2 + D^2}$

Graph is showing proportional contribution of each components to on product overlay

Matched machine overlay on resist on silicon	6 nm	4.5 nm	3.5 nm	3 nm	2.5 nm
Application specific lot control	3 nm	2 nm	1.5 nm	1.5 nm	1 nm
Application specific process contribution	5 nm	3.5 nm	2.5 nm	1.5 nm	1 nm
Reticle writing error	1.5 nm	1.5 nm	1 nm	1 nm	1 nm

Holistic approach required to reduce overlay



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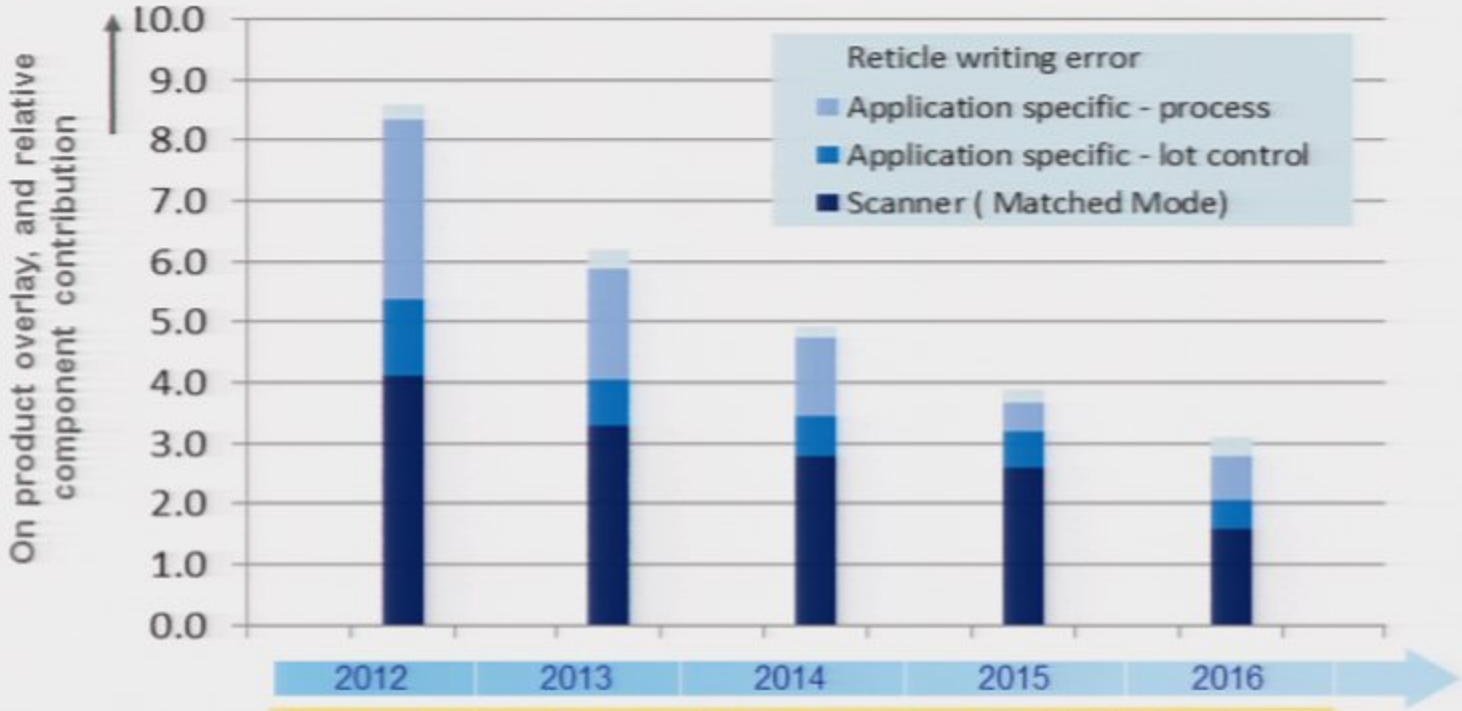
Matched machine overlay on resist on silicon	6 nm	4 nm	Scanner improvement		2.5 nm
Application specific lot control	3 nm	2 nm	1.5 nm	1.5 nm	1 nm
Application specific process contribution	5 nm	3.5 nm	2.5 nm	1.5 nm	1 nm
Reticle writing error	1.5 nm	1.5 nm	1 nm	1 nm	1 nm

Holistic approach required to reduce overlay



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Reticle writing error	1.5 nm	1.5 nm	1 nm	1 nm	1 nm

Scanner improvement

Integrated metrology and feedback loop

Litho performance, process window size & control

The trinity in a holistic litho approach

Stepper set up and layout optimization for maximum process window

Stepper control through on-product overlay, focus and CD feedback loops window

1. Advanced lithography capability
(Imaging, overlay and focus)

2. Process window enlargement

Parameterize control loops and thresholds

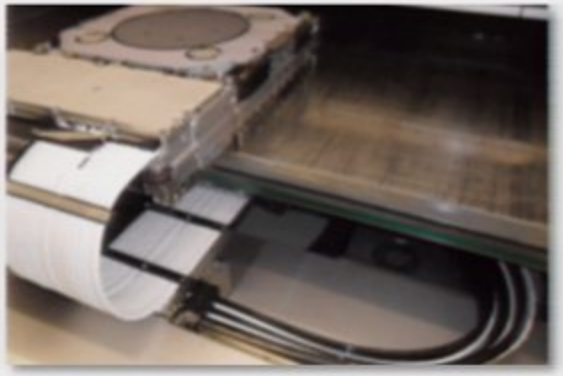
3. Process window control

1) Next immersion platform to support 2014 requirements

Enabling cost effective double patterning

NXT:1970Ci Improvement	Overlay (DCO/MMO/ lens heating)	Focus control (Uniformity/ stability/ lens heating)	Productivity (Throughput/Lot Overhead/ Availability)
	3.5 nm -20%	20 nm -15%	250 Wfrs/hr +10%
Stage design	✓	✓	✓
Projection lens	✓		✓
Focus sensor		✓	✓
Image sensors	✓		✓

Focus sensor

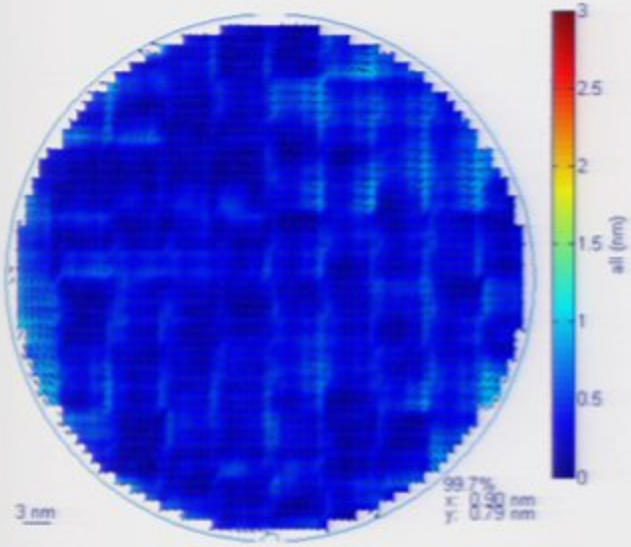


wafer stage

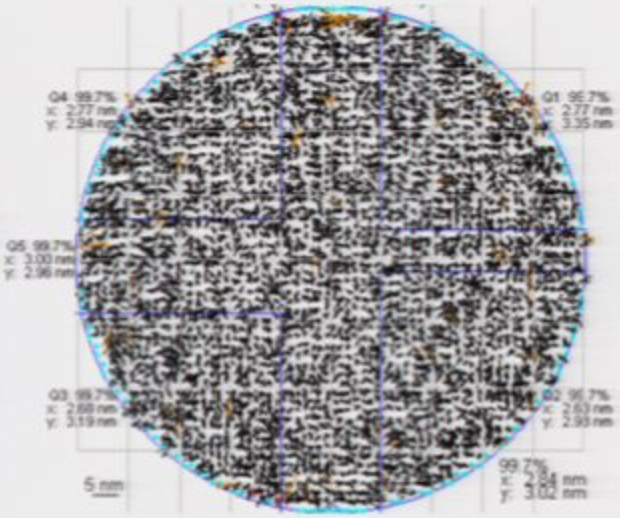
overlay and Image sensors

DCO – Dedicated Chuck Overlay MMO – Matched Machine Overlay

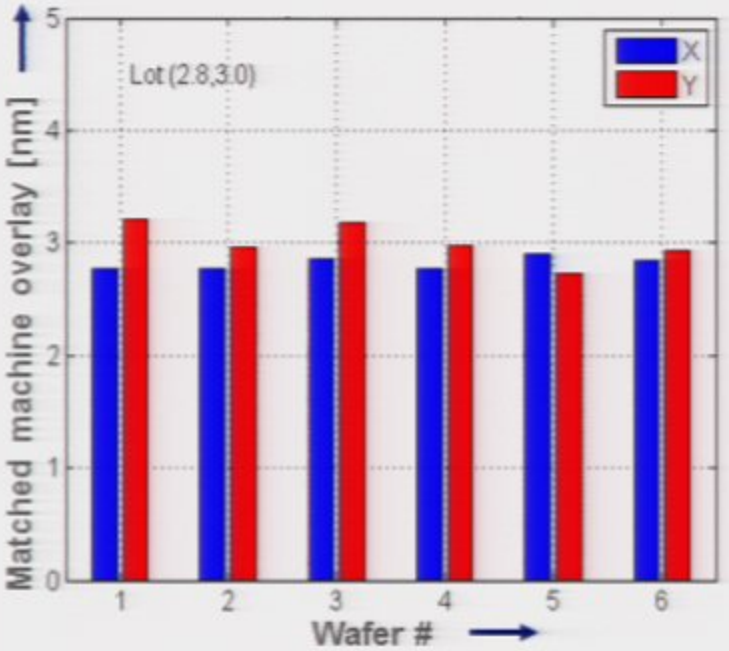
1) Full wafer system overlay performance to < 3 nm



Dedicated chuck
full wafer overlay <1 nm

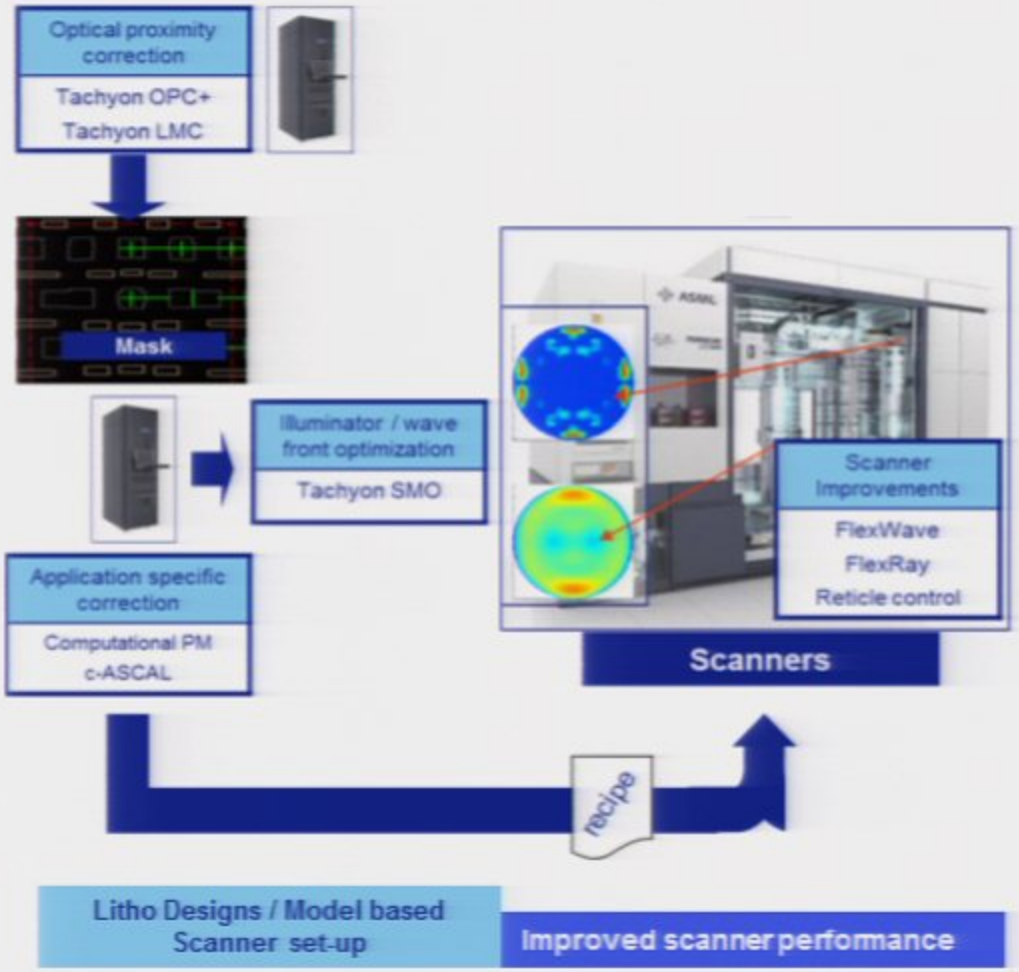


Matched machine
full wafer overlay 3 nm



Multiple wafers
matched machine
full wafer overlay 3 nm

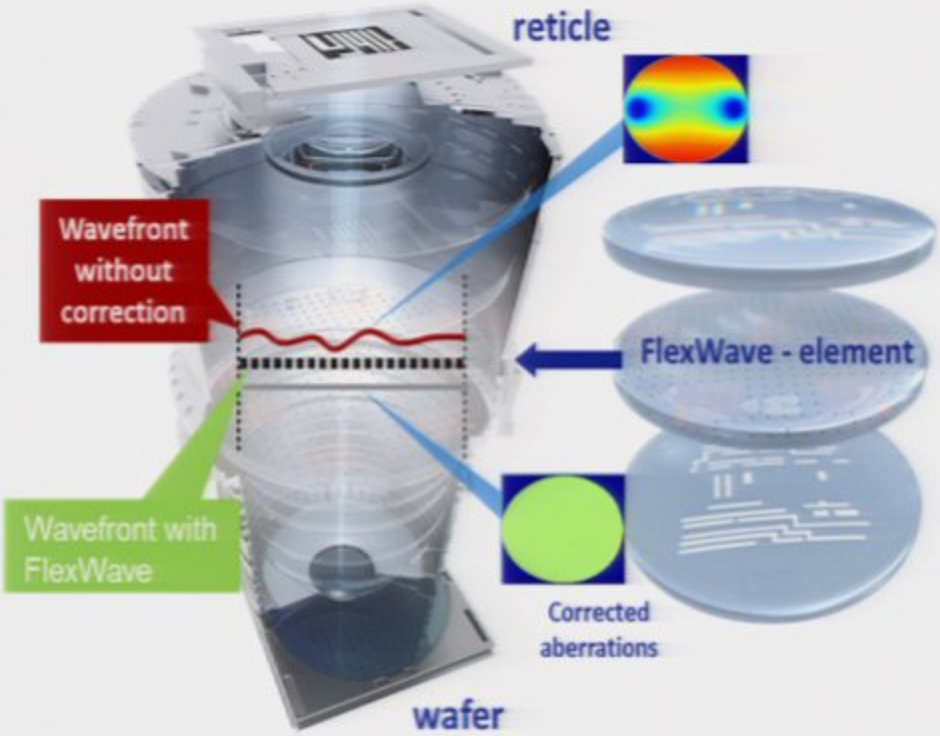
2) Widen the process window to increase budget

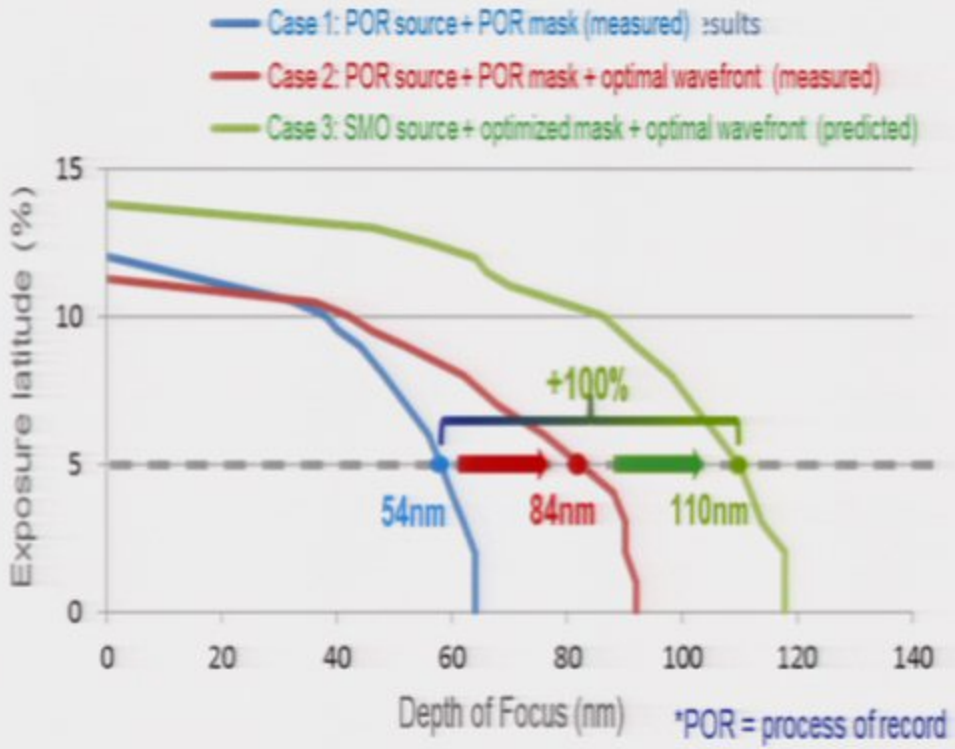


Process window enlargement

2) 2x process window with full Litho-Mask tuning

Full source-mask-wave front optimization solving mask 3D problem

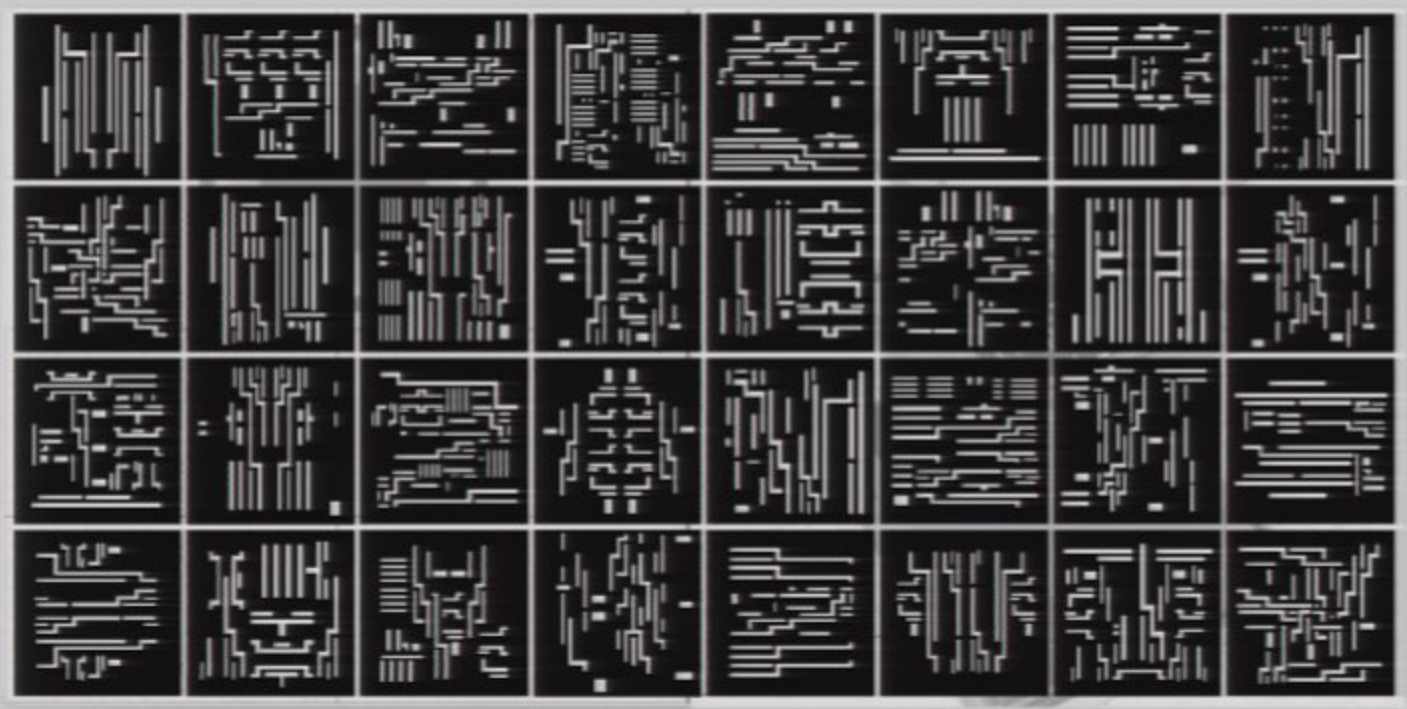




- Wave Front only flow (Case 2) shows 56% improvement in overlapping process window
- Full flow (Case 3) prediction shows doubling the overlapping process window, to be proven by measurements

2) Flexible Mask Optimization, the next step

in Optical Proximity Correction (OPC)



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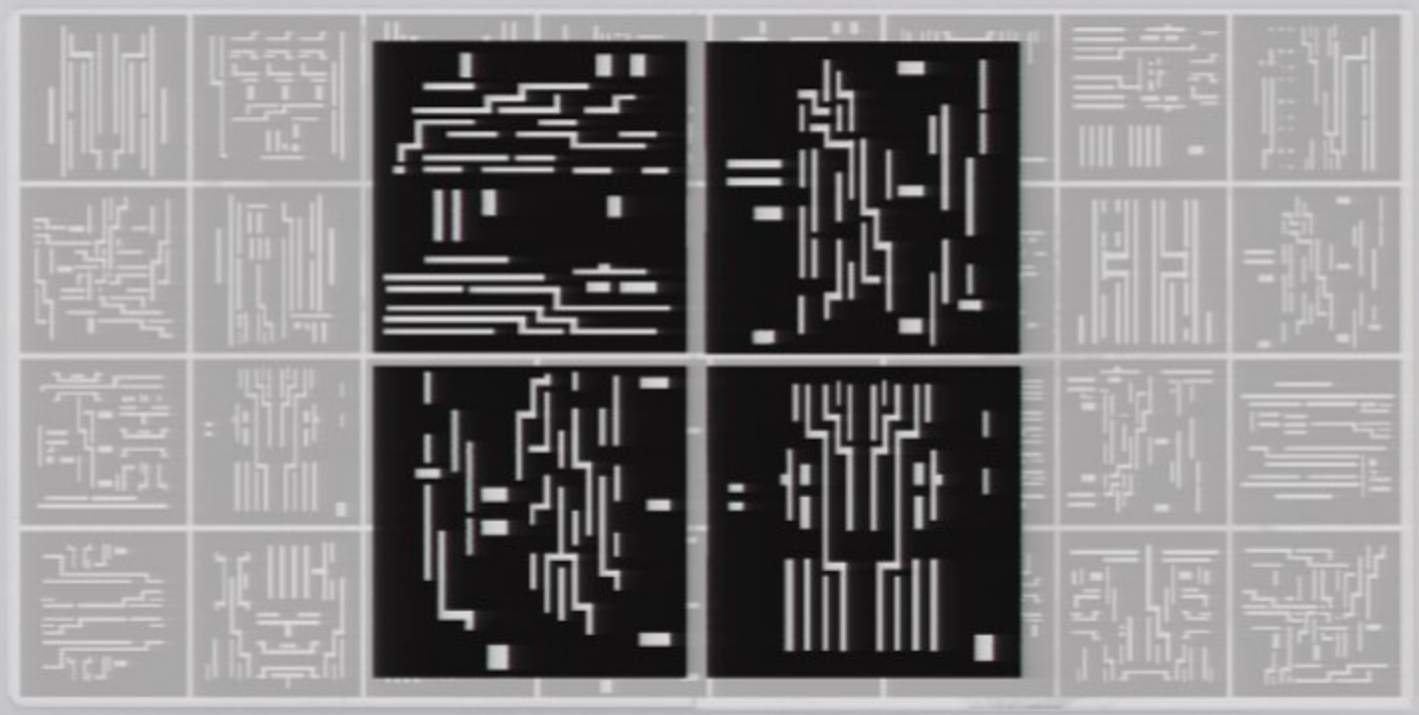
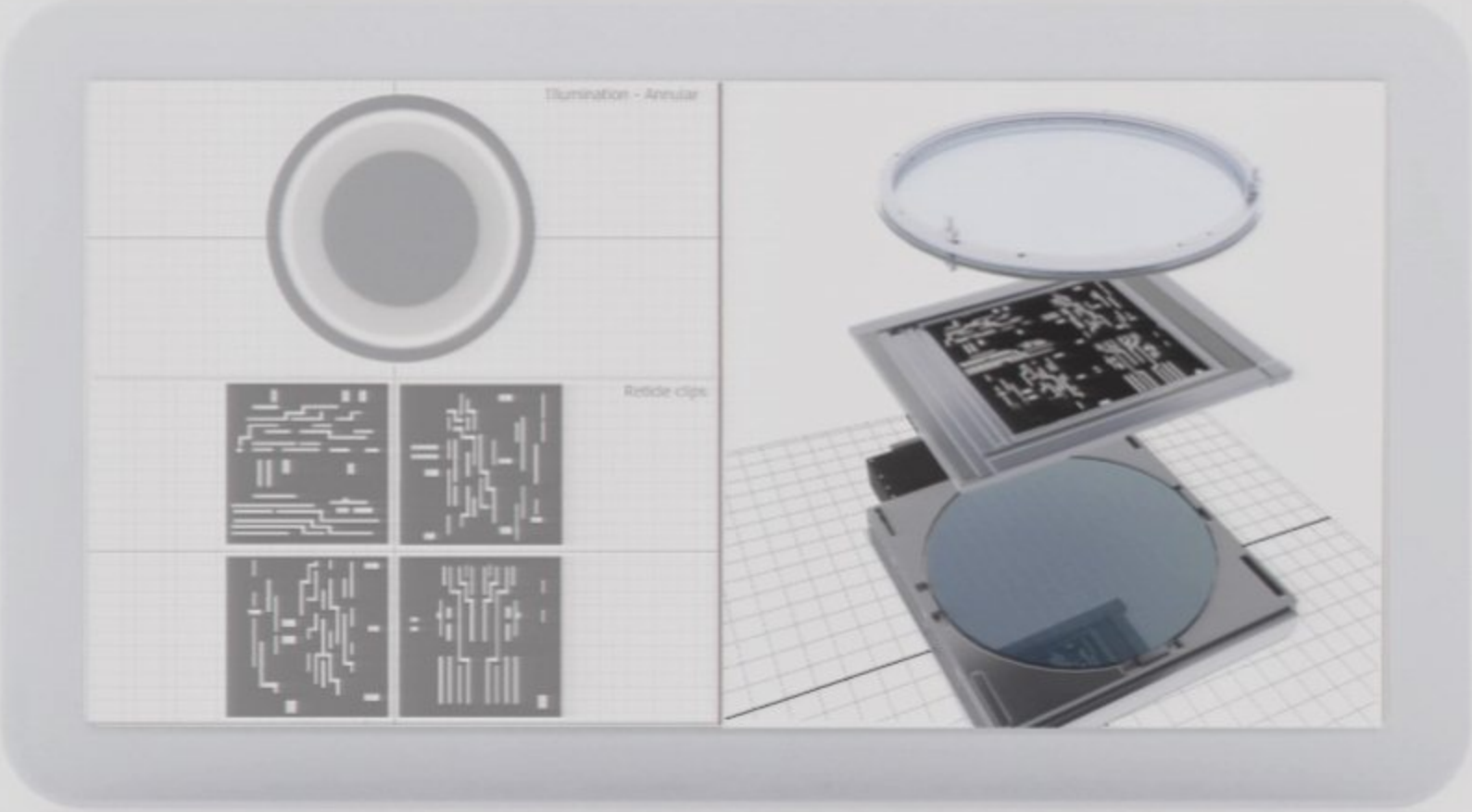


Select design clips that represent known critical patterns for layer, node and application

2) Flexible Mask Optimization, the next step

in Optical Proximity Correction (OPC)



Critical layers in current devices cannot be imaged without OPC

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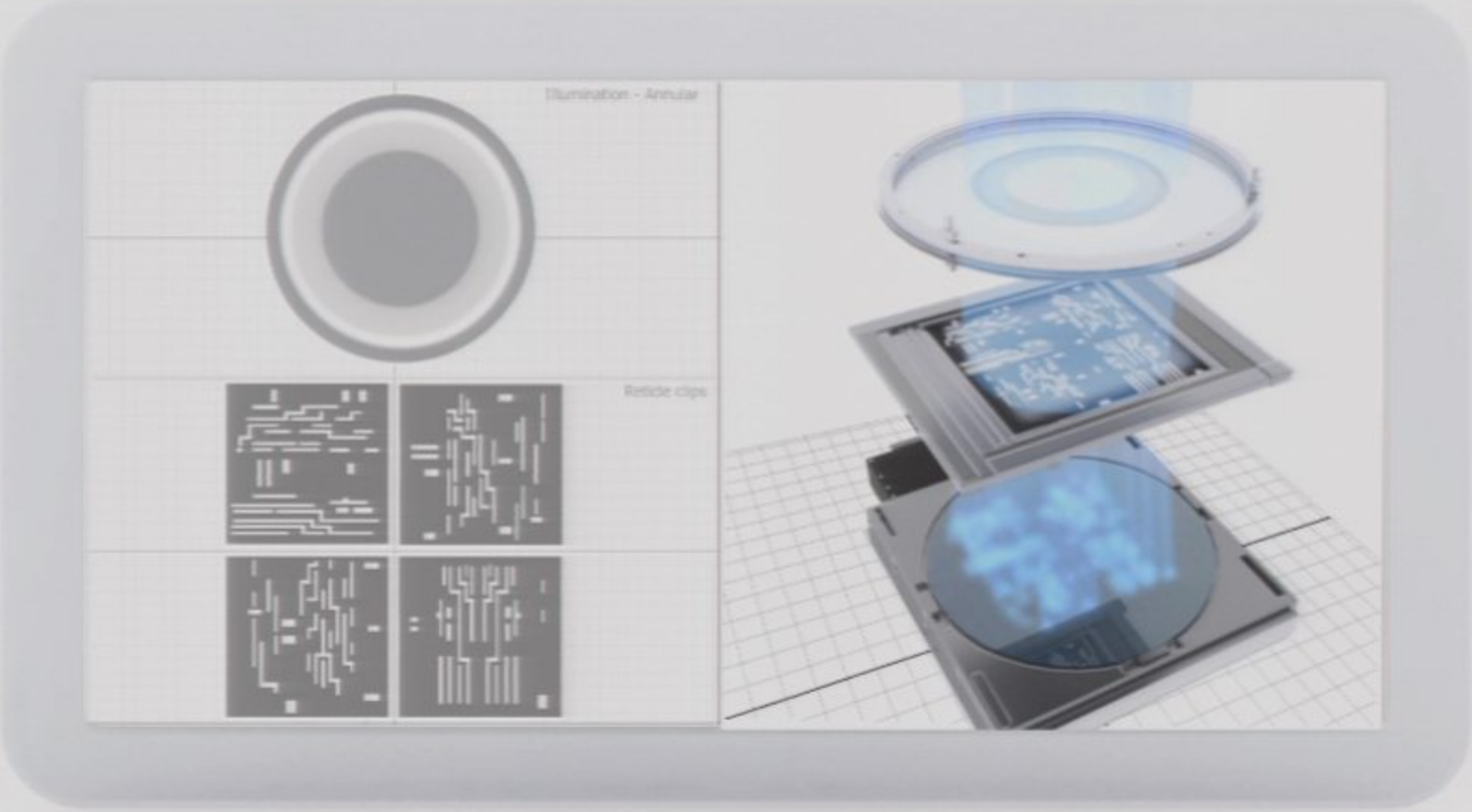

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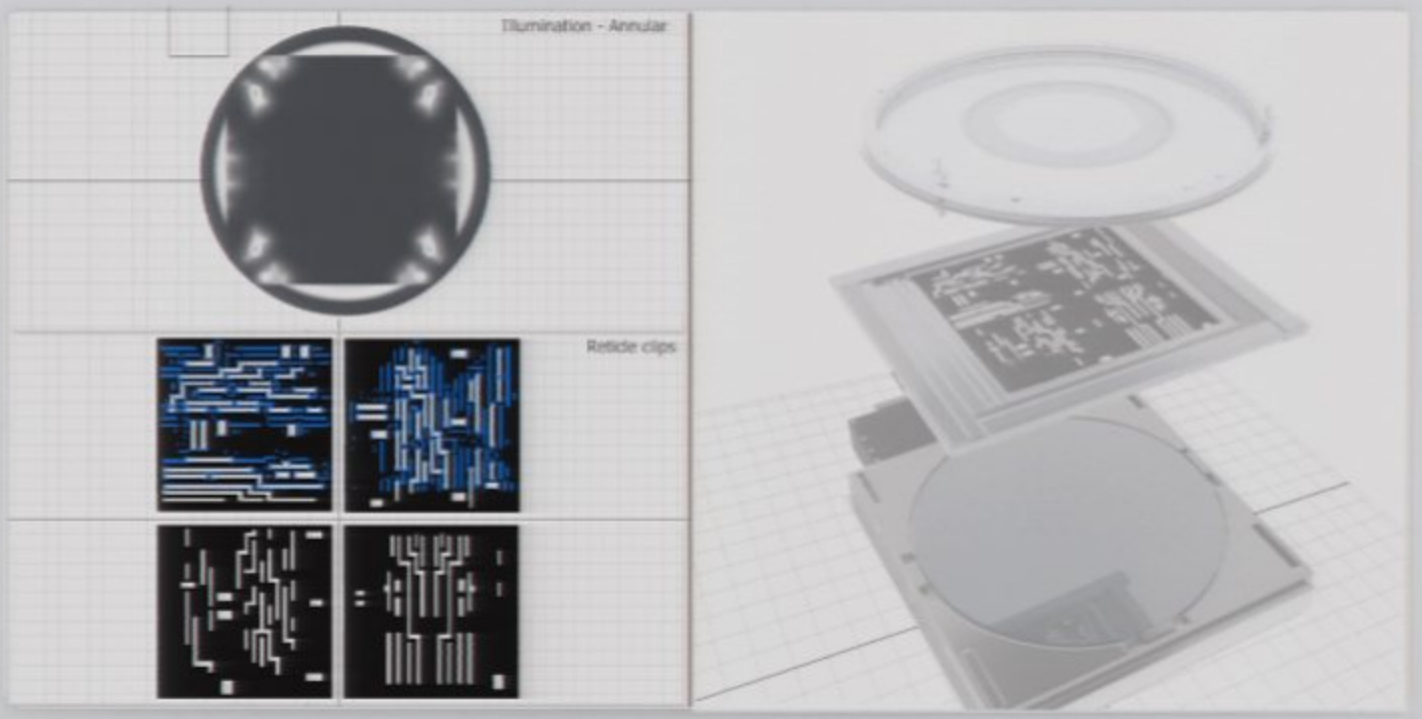
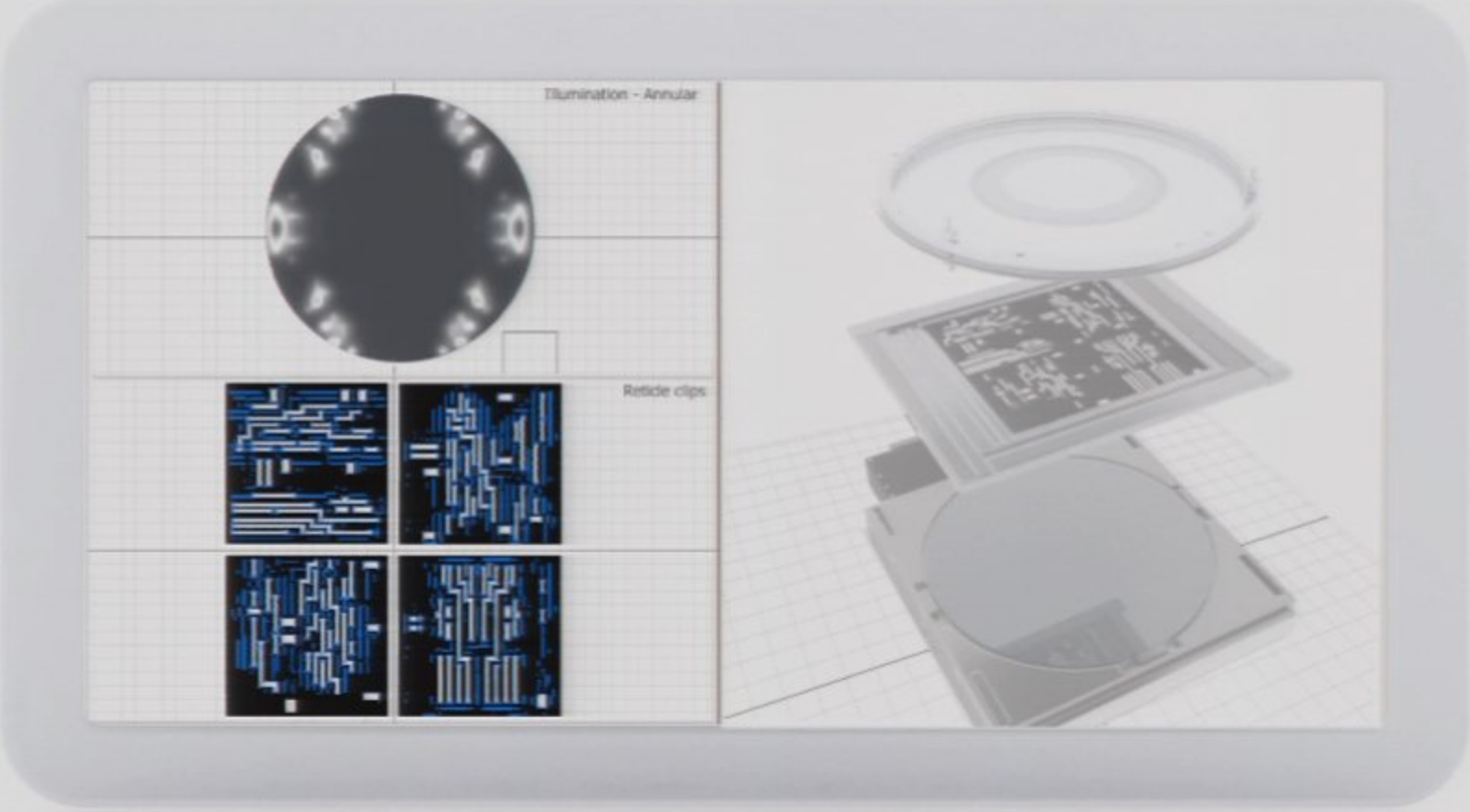


Co-optimizing OPC and source

2) Flexible Mask Optimization, the next step

in Optical Proximity Correction (OPC)



Co-optimizing OPC and source

2) Flexible Mask Optimization, the next step
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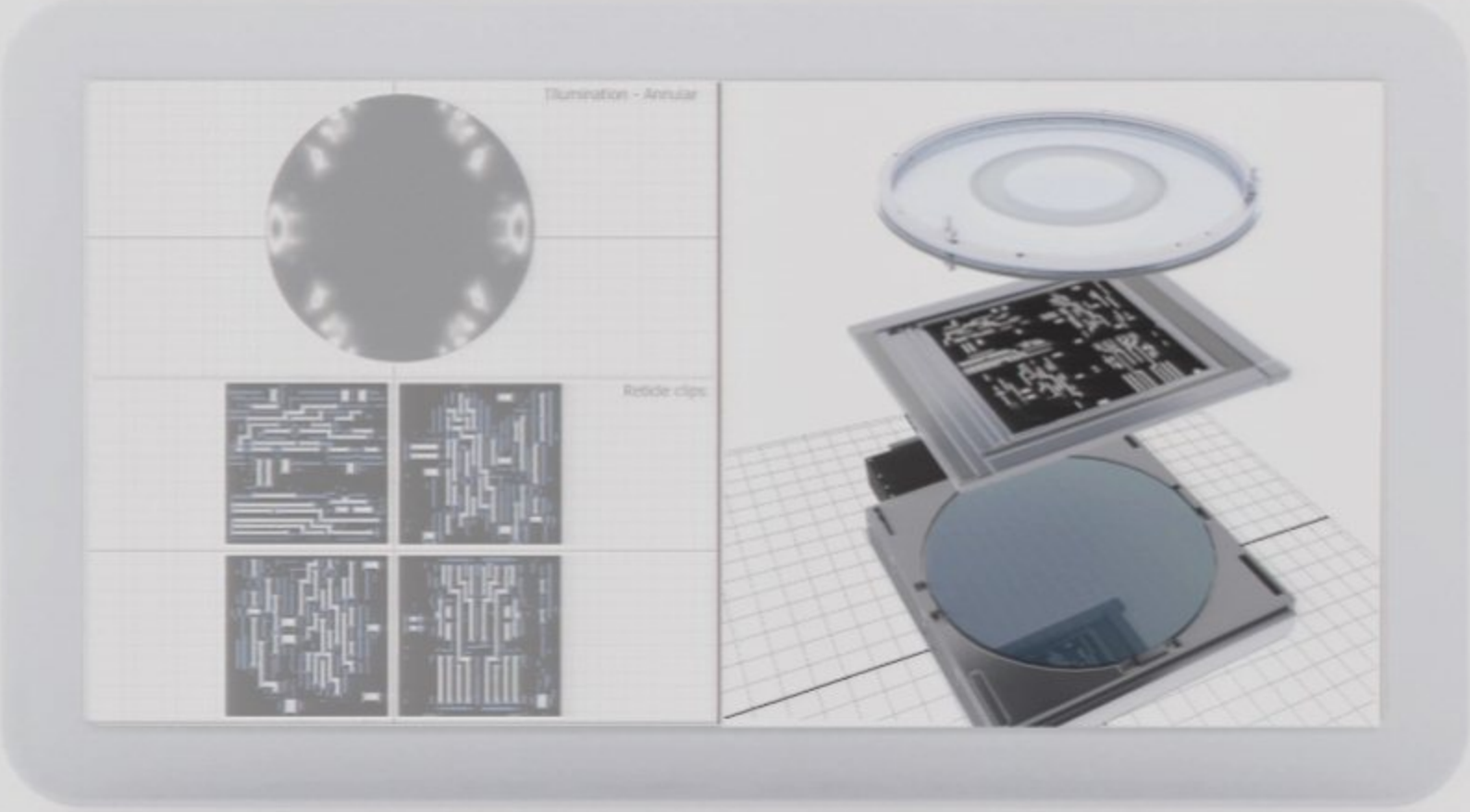

Co-optimizing OPC and source resu

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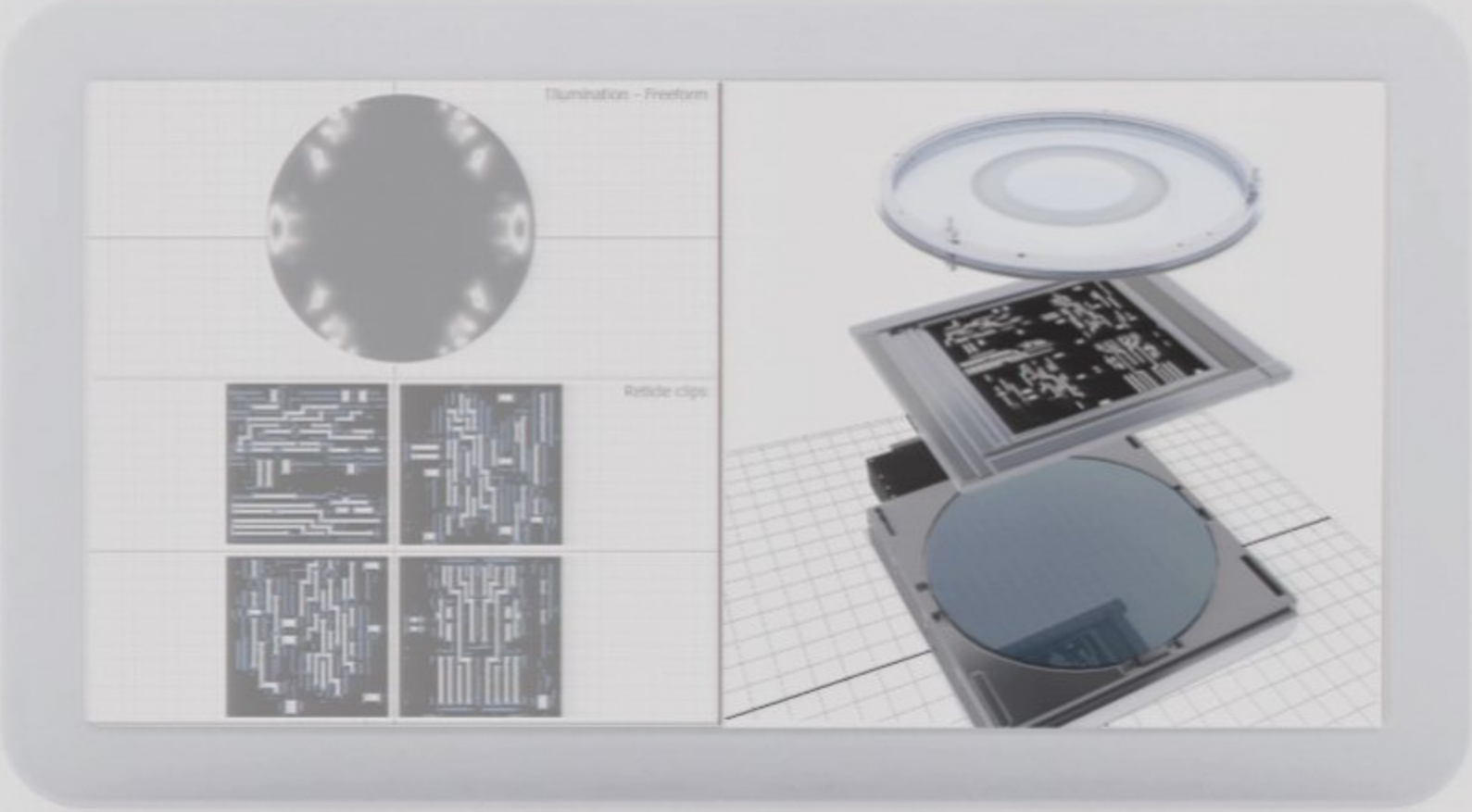
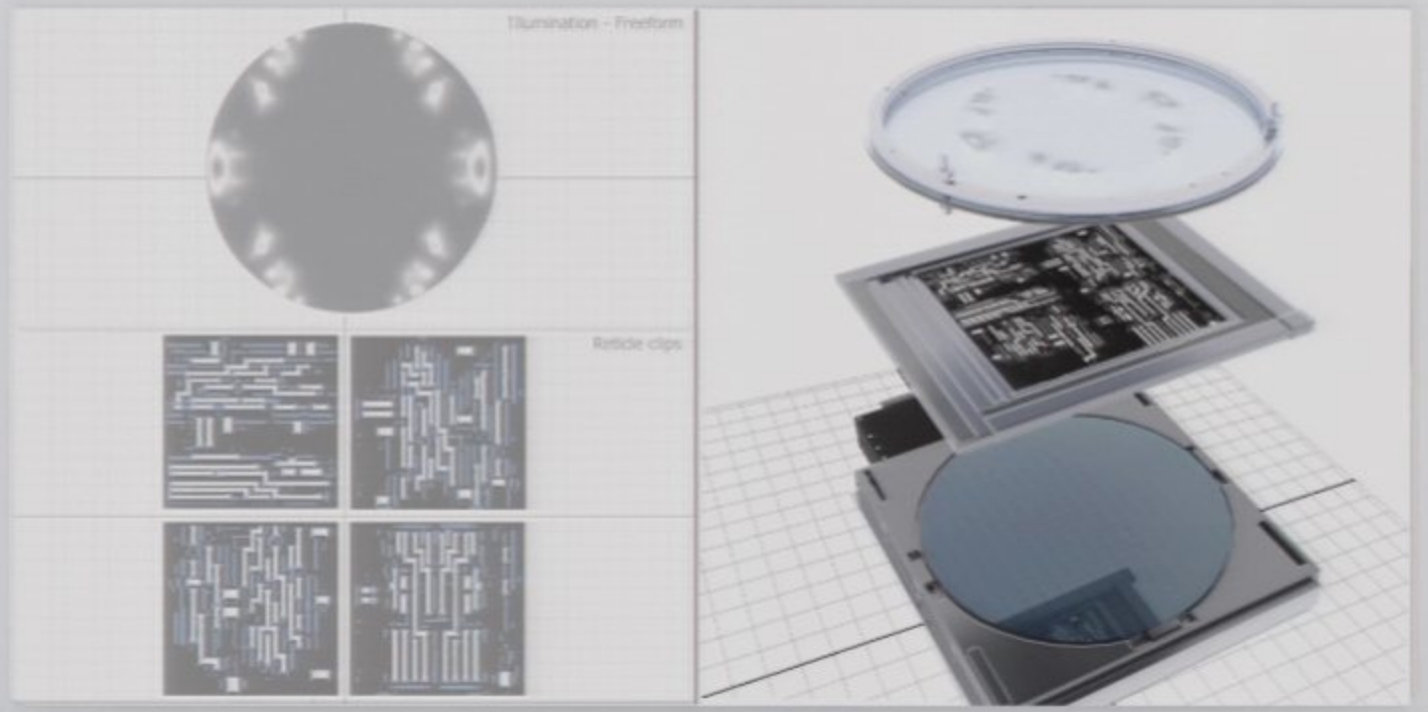


Co-optimizing OPC and source results in optimal imaging

2) Flexible Mask Optimization, the next step

in Optical Proximity Correction (OPC)



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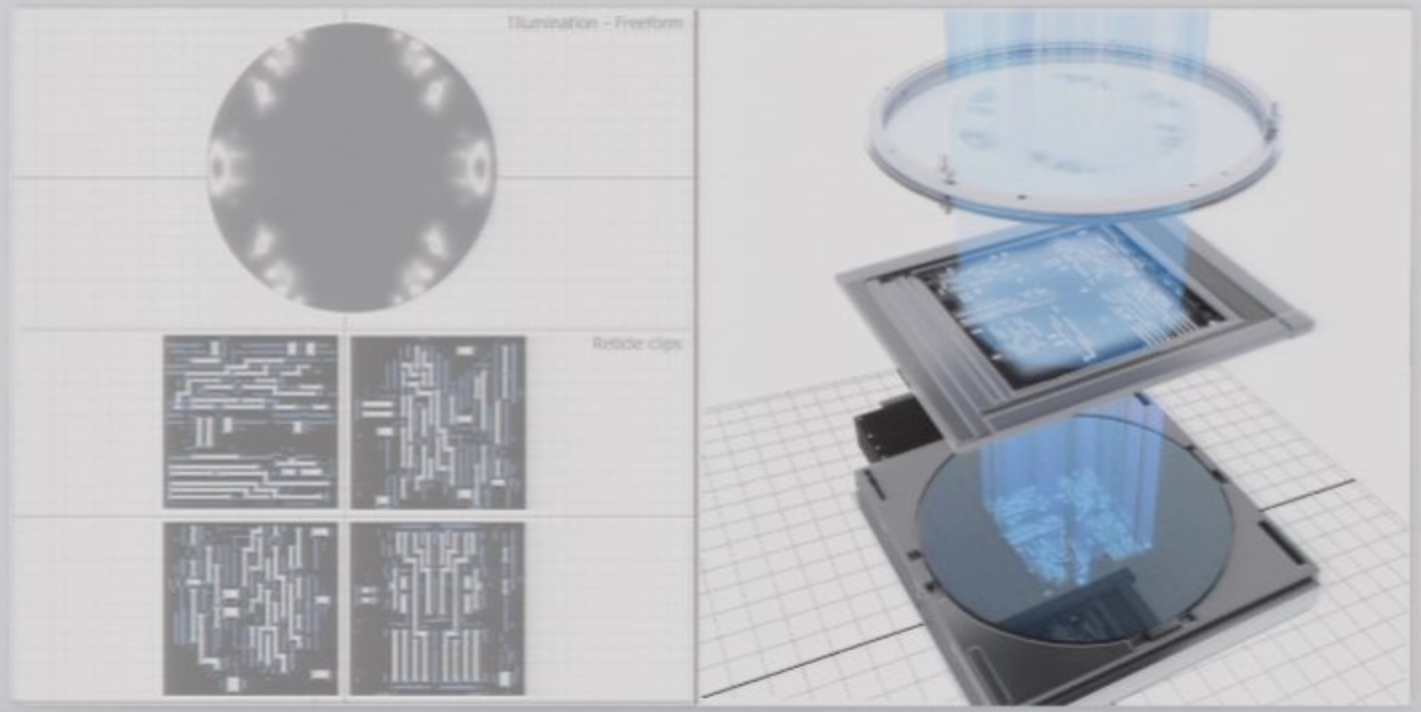

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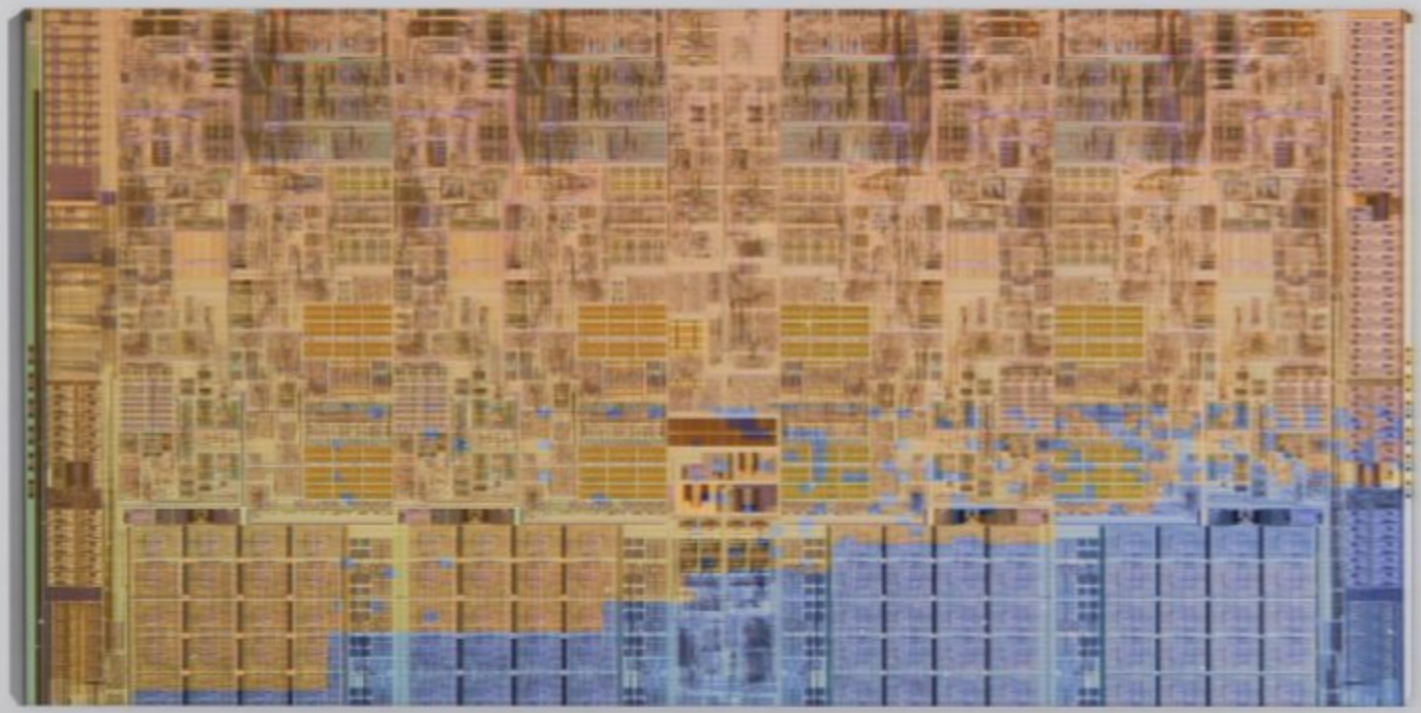
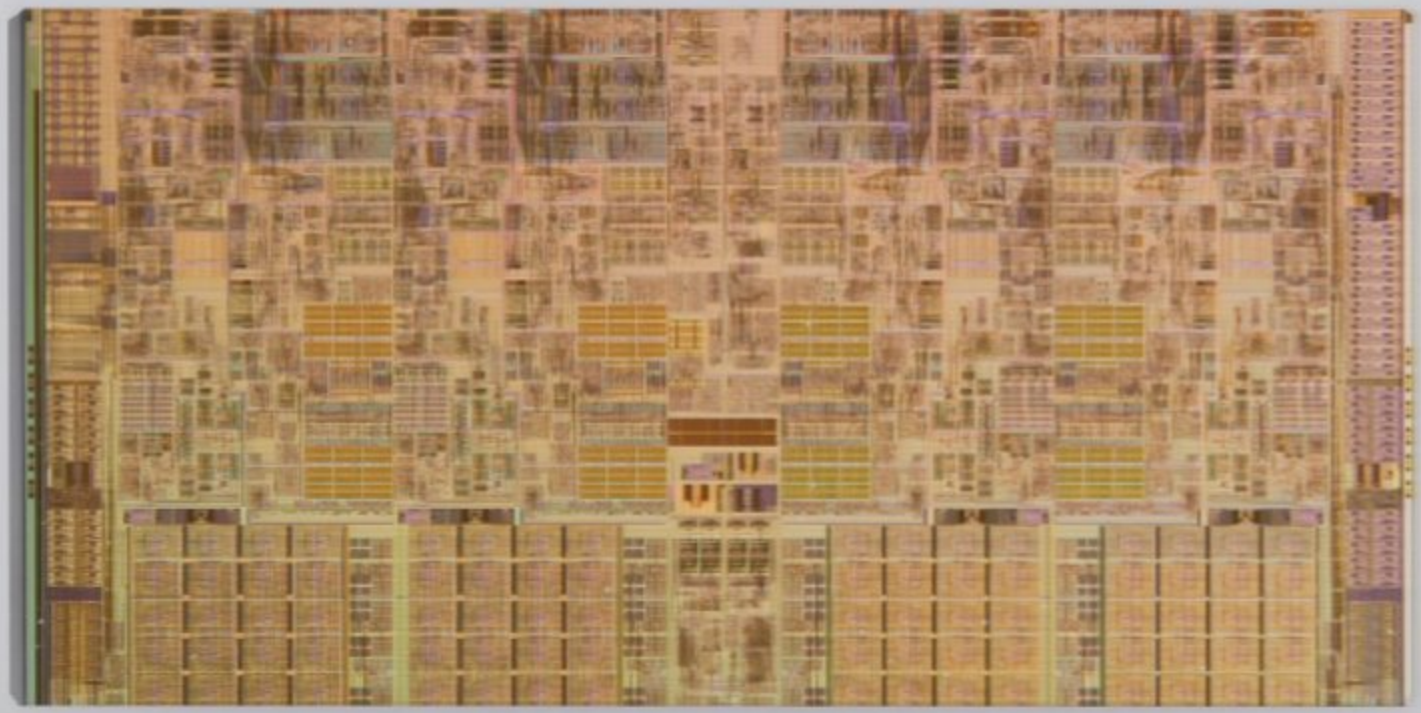


Perform OPC on full chip and verify full chip

2) Flexible Mask Optimization, the next step

in Optical Proximity Correction (OPC)



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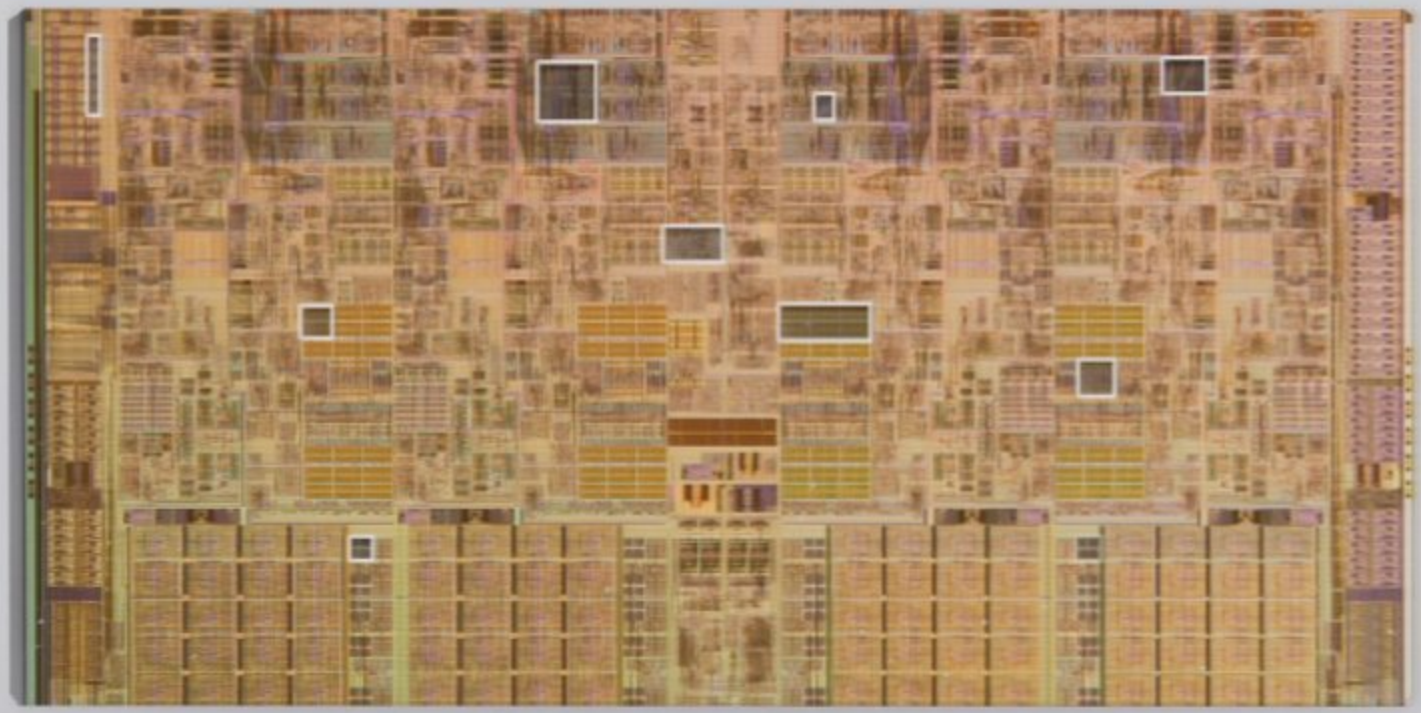
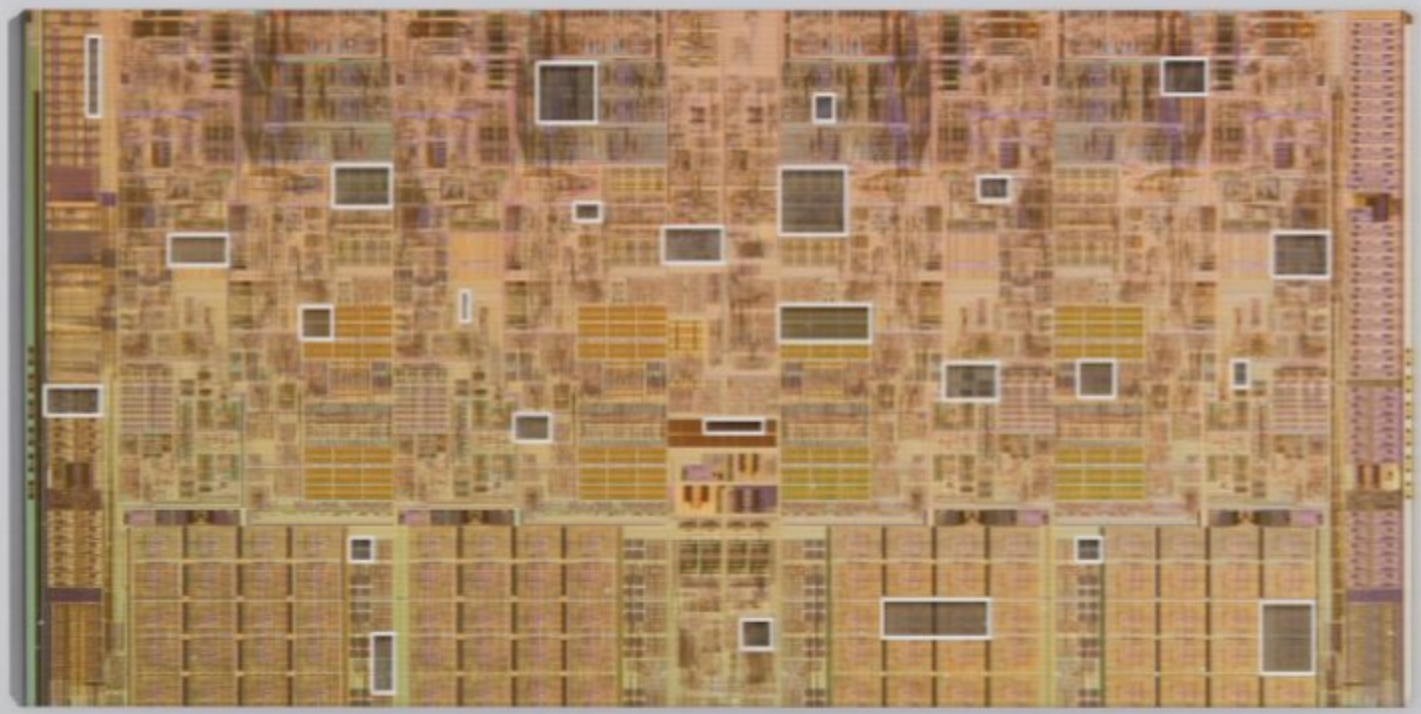


Determine chip specific process window hotspots

2) Flexible Mask Optimization, the next step

in Optical Proximity Correction (OPC)



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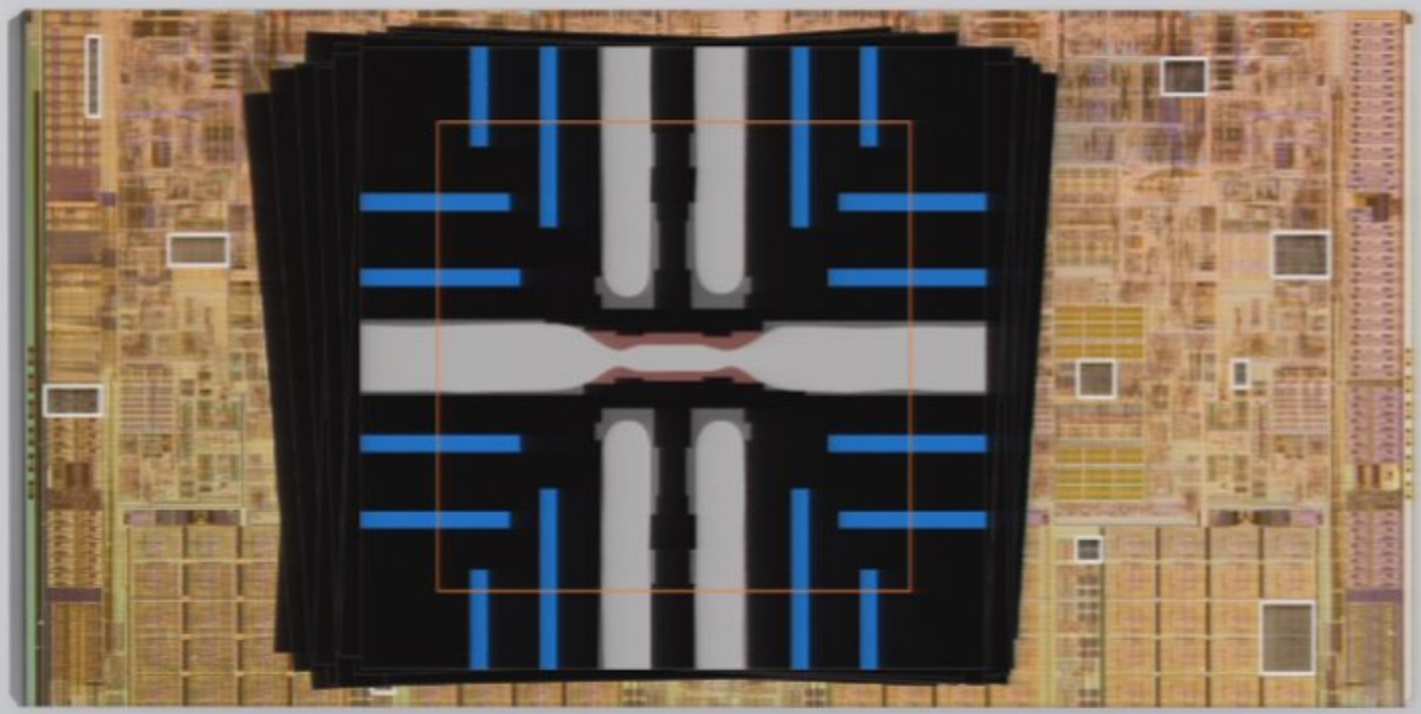

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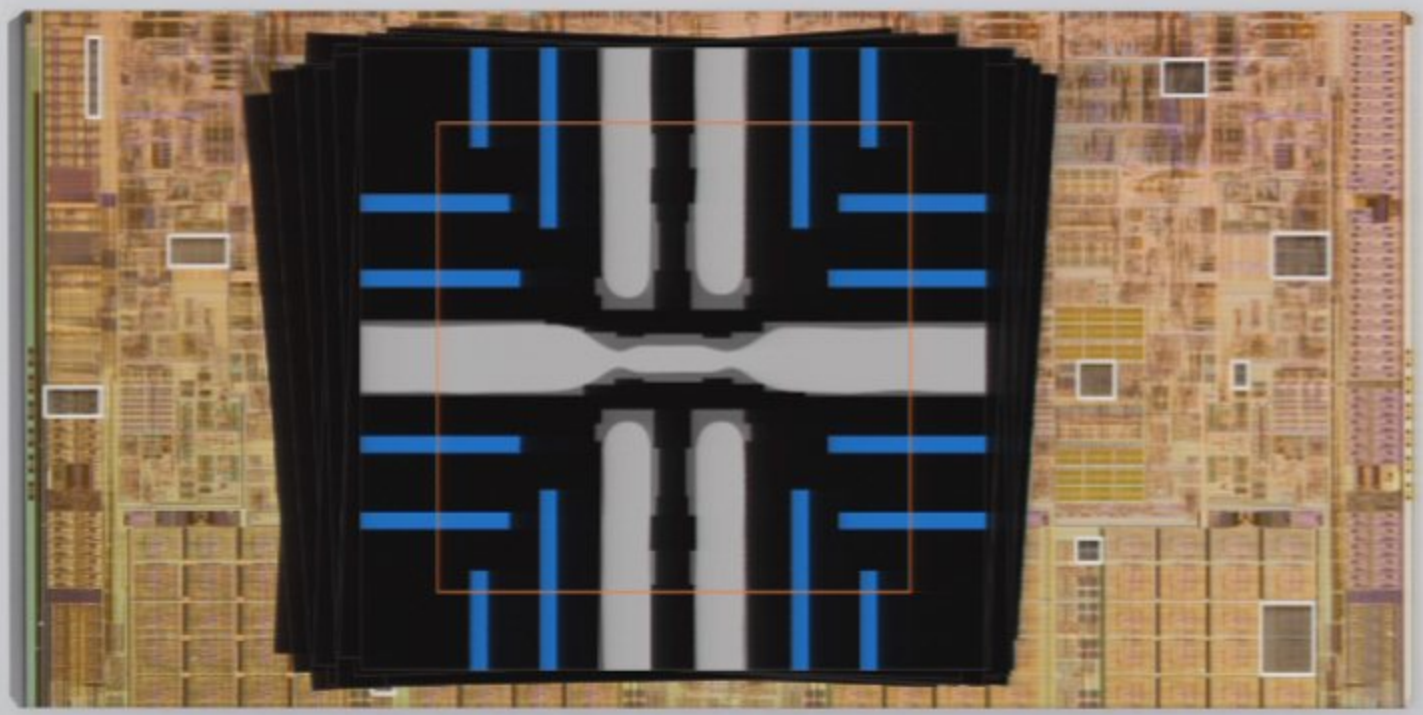
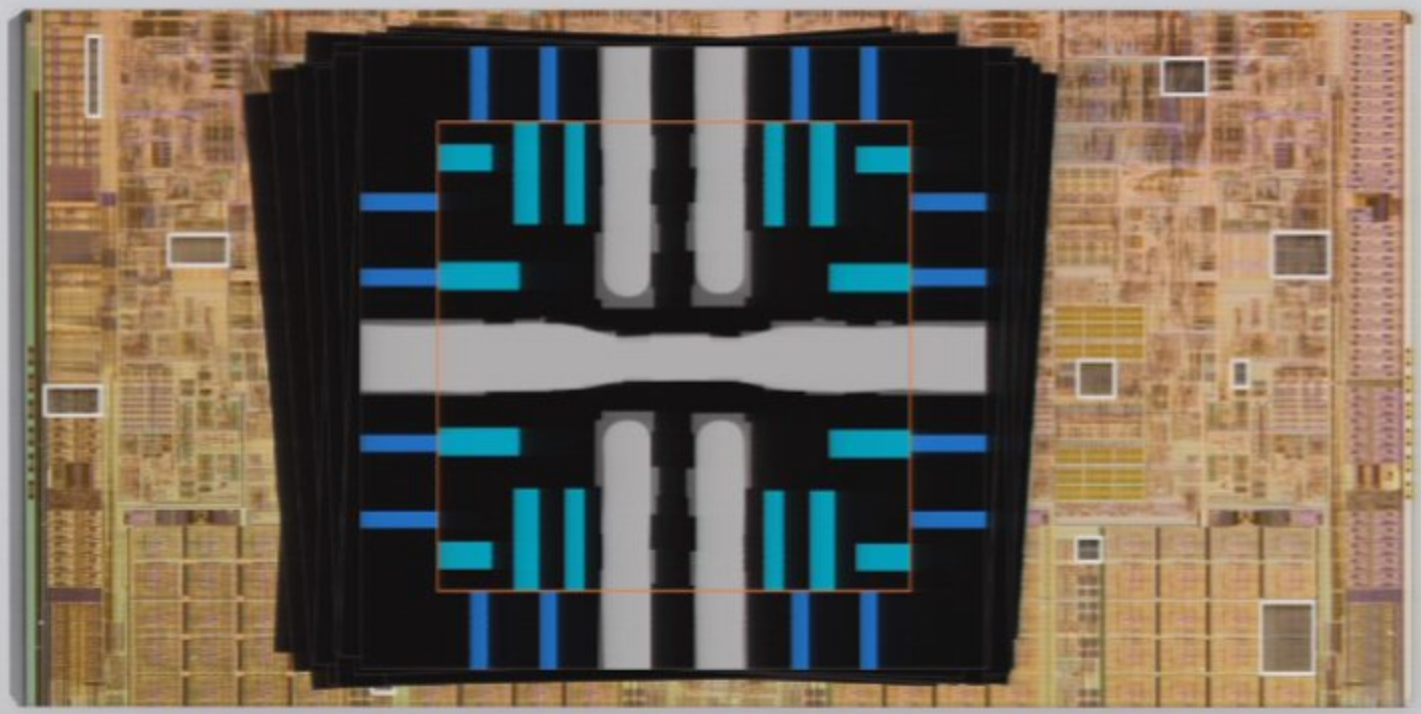


Optimize hotspots using advanced OPC techniques

2) Flexible Mask Optimization, the next step

in Optical Proximity Correction (OPC)



Boundary healing

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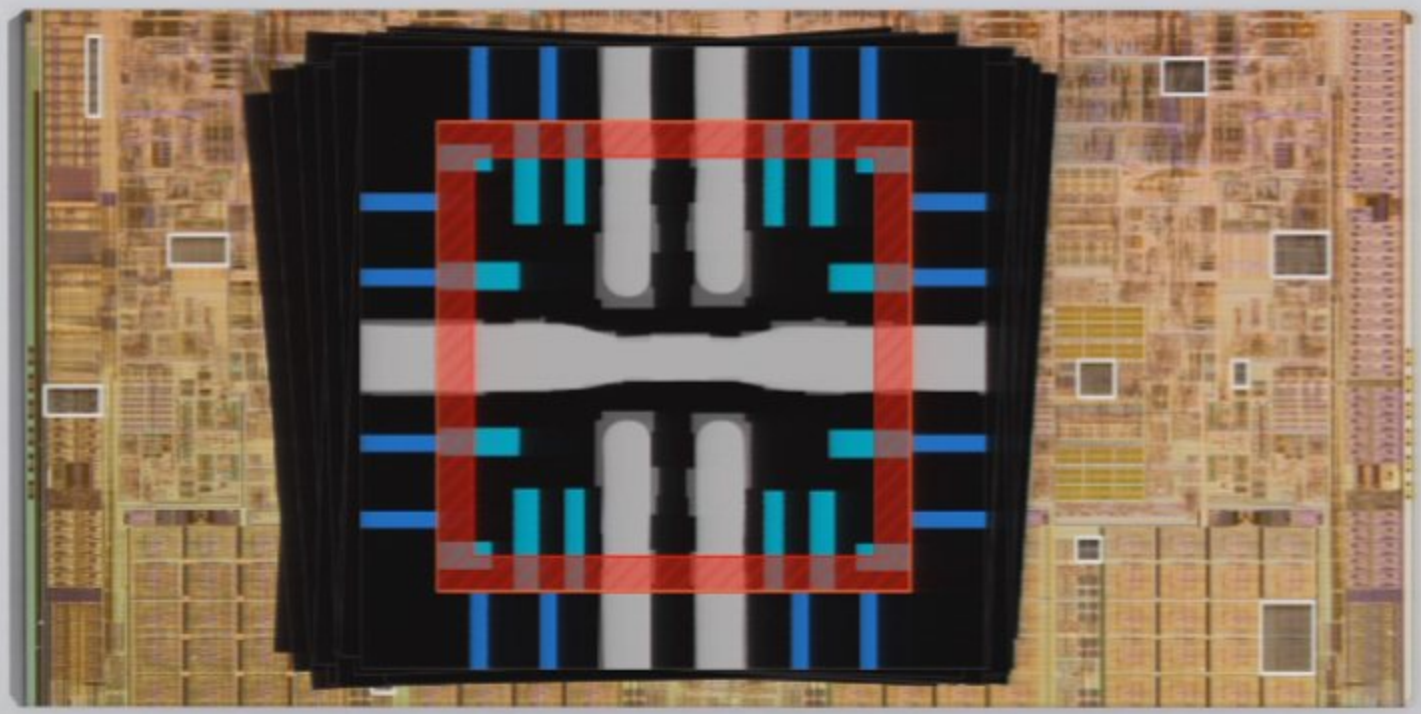

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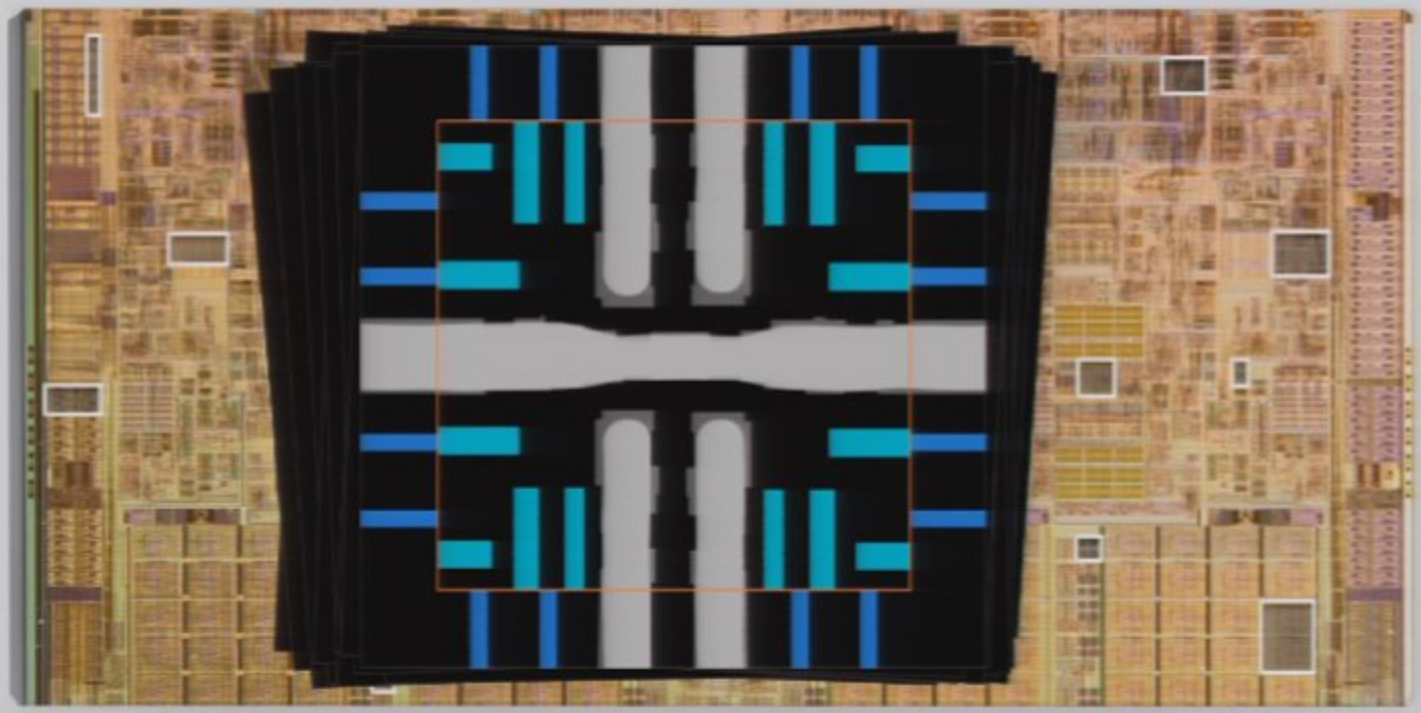

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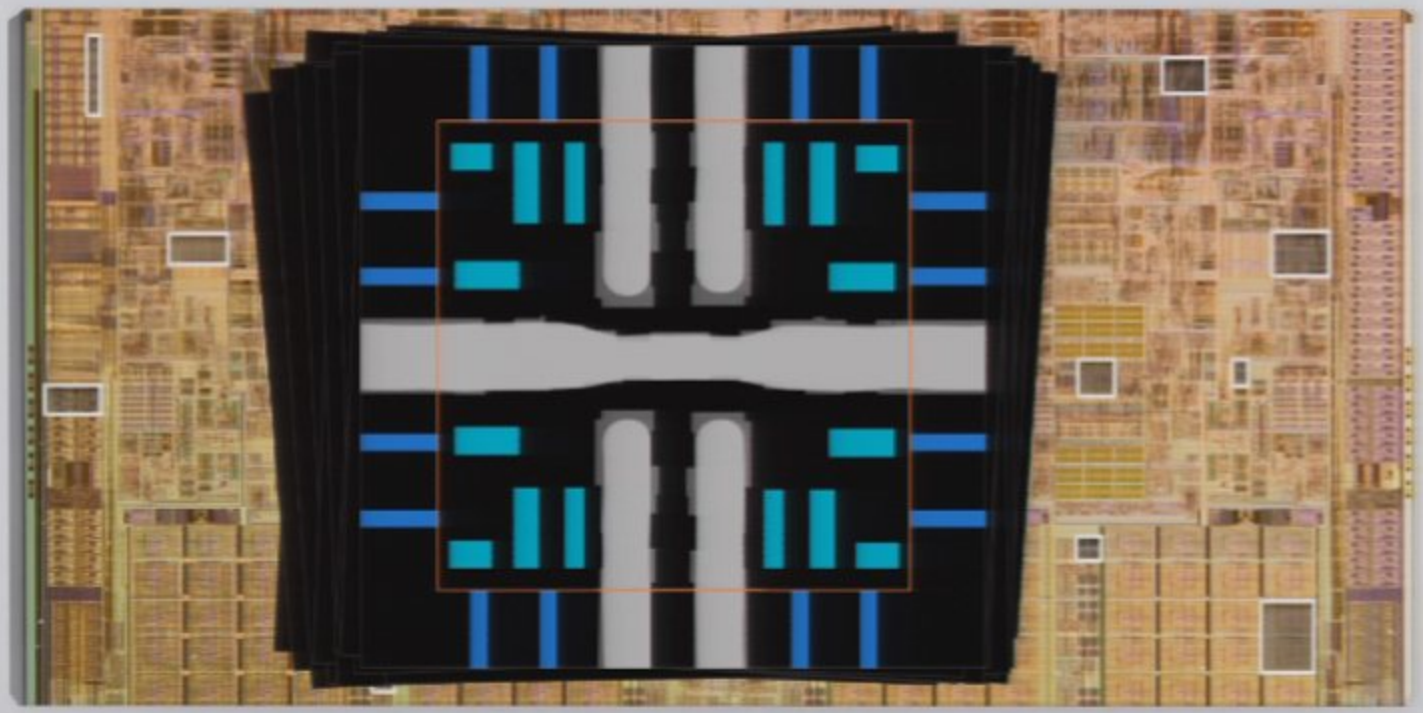

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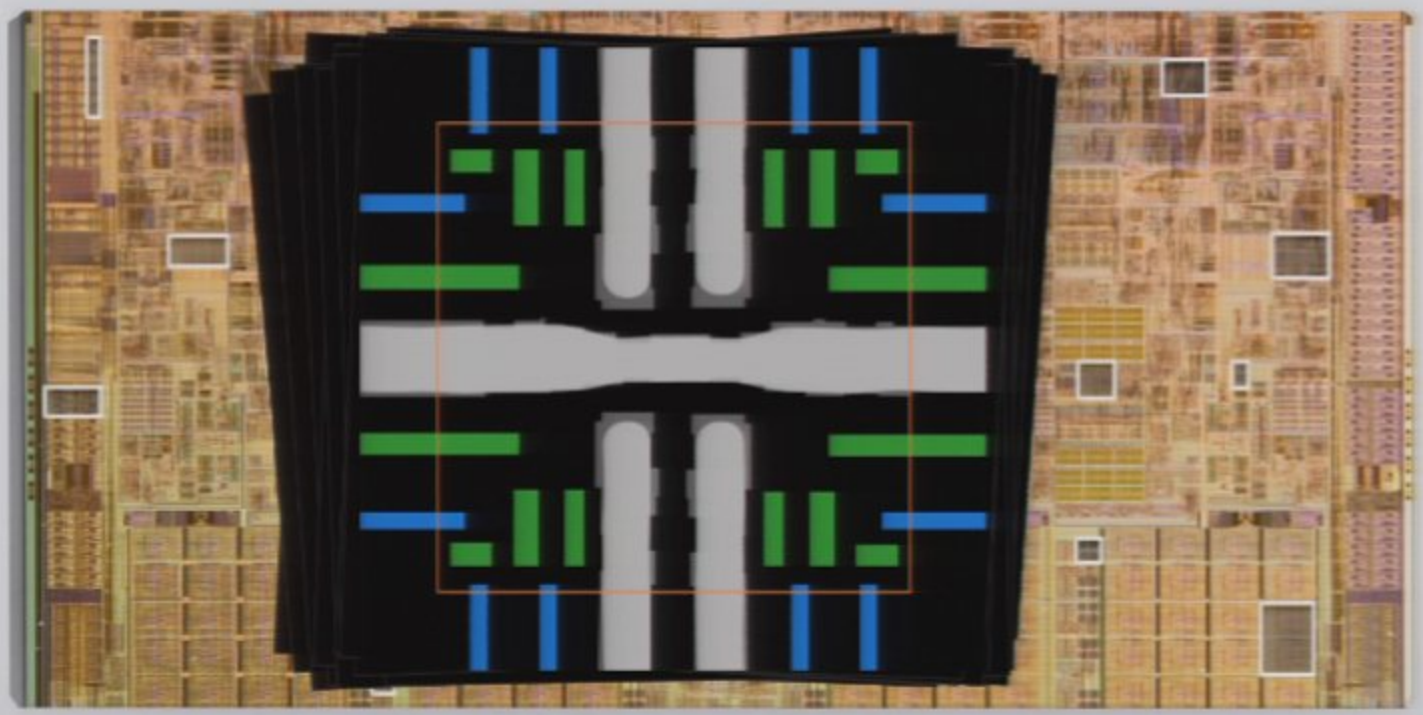

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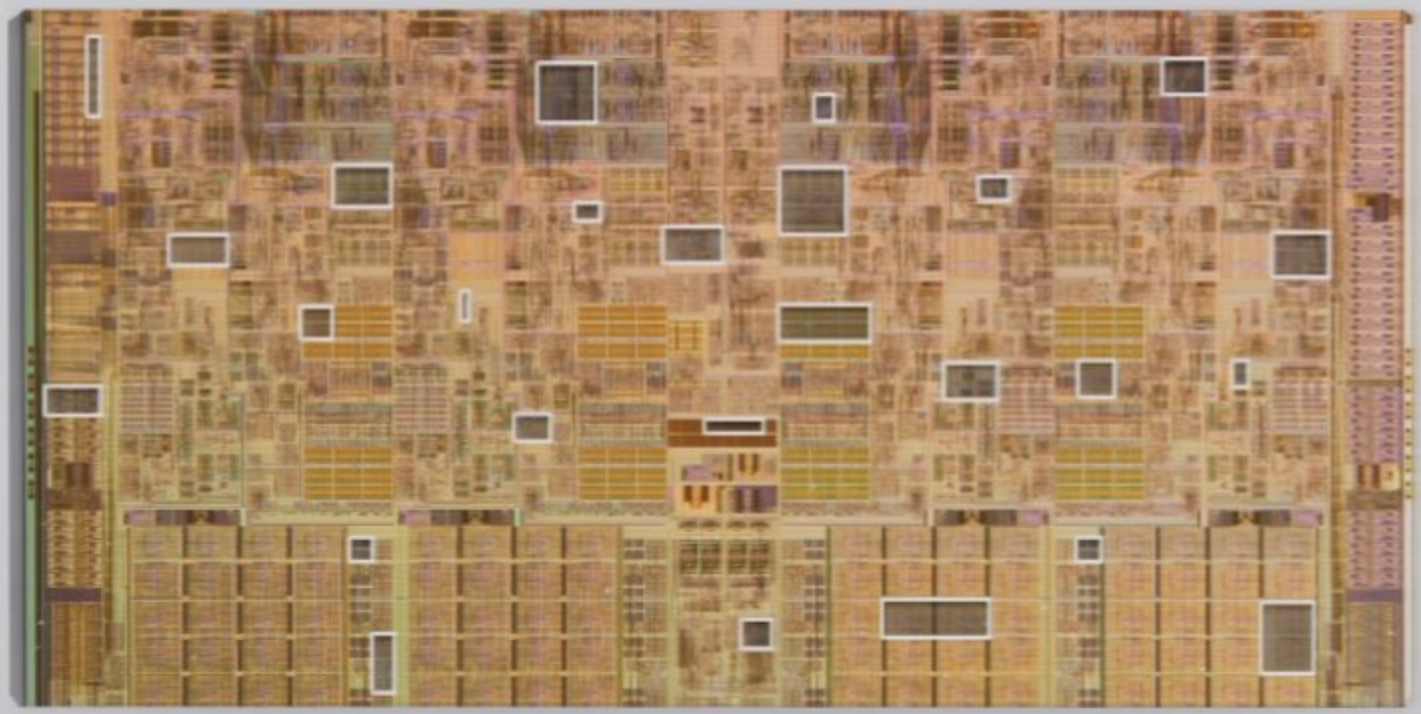

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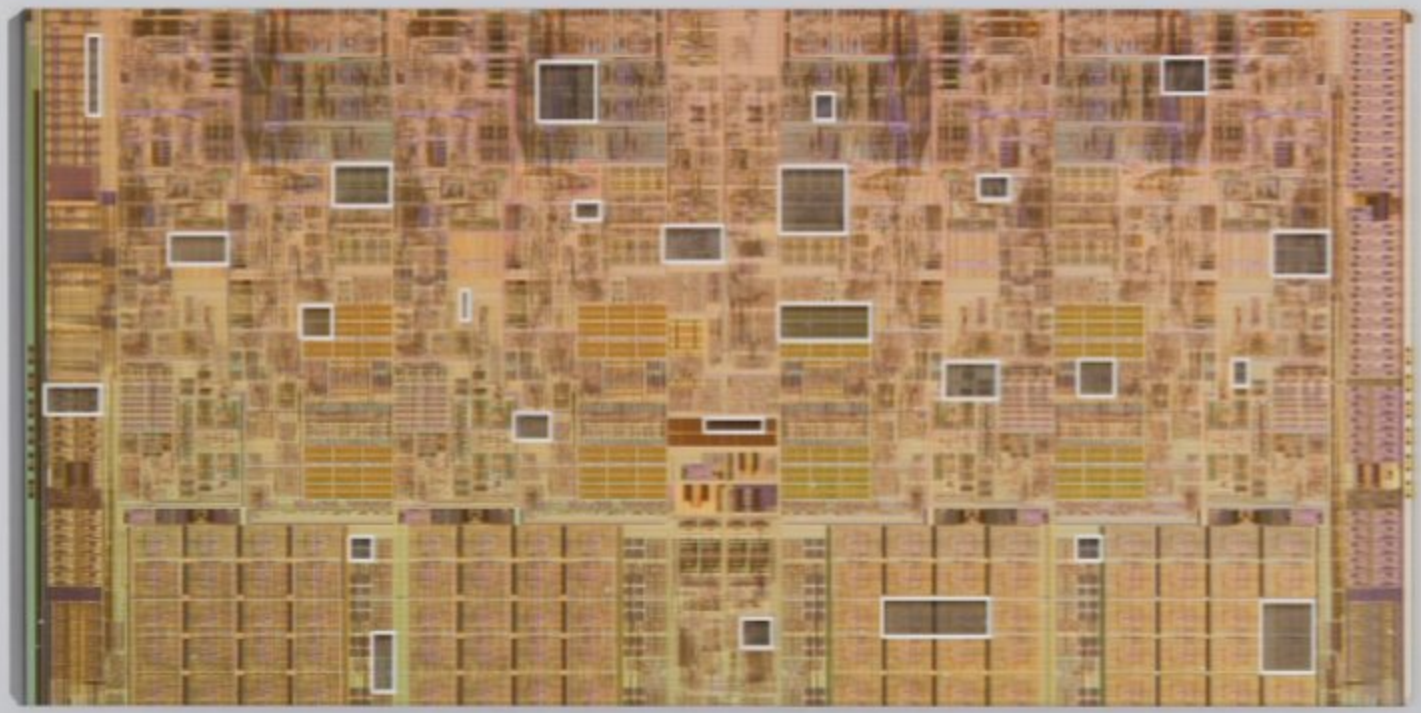
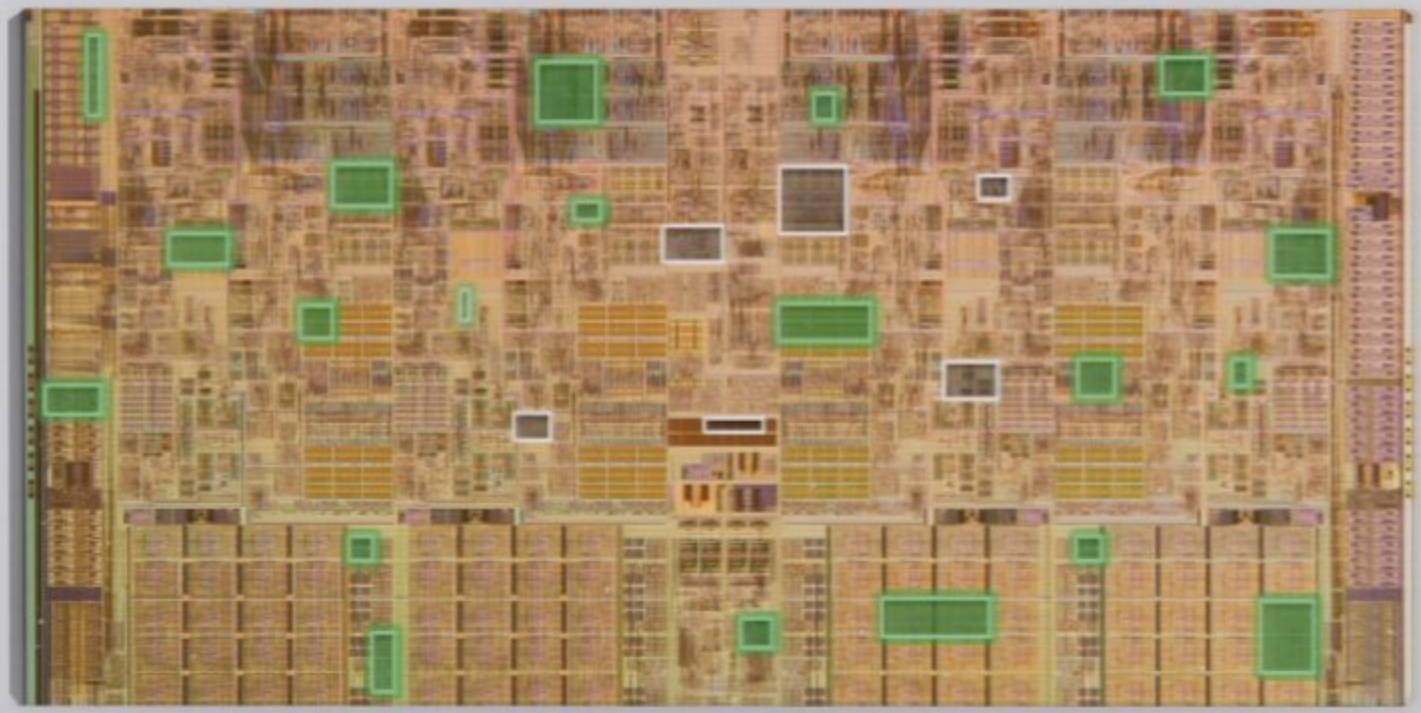


Final verification

2) Flexible Mask Optimization, the next step

in Optical Proximity Correction (OPC)



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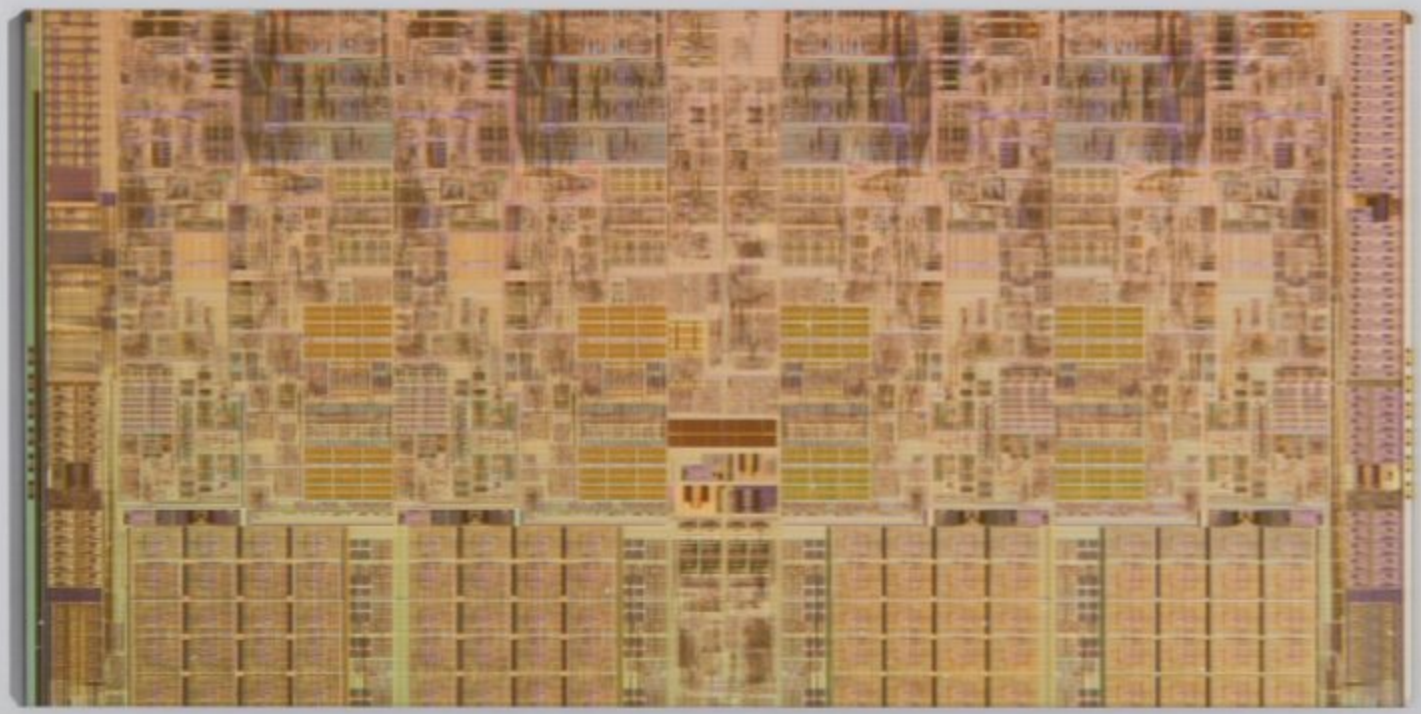

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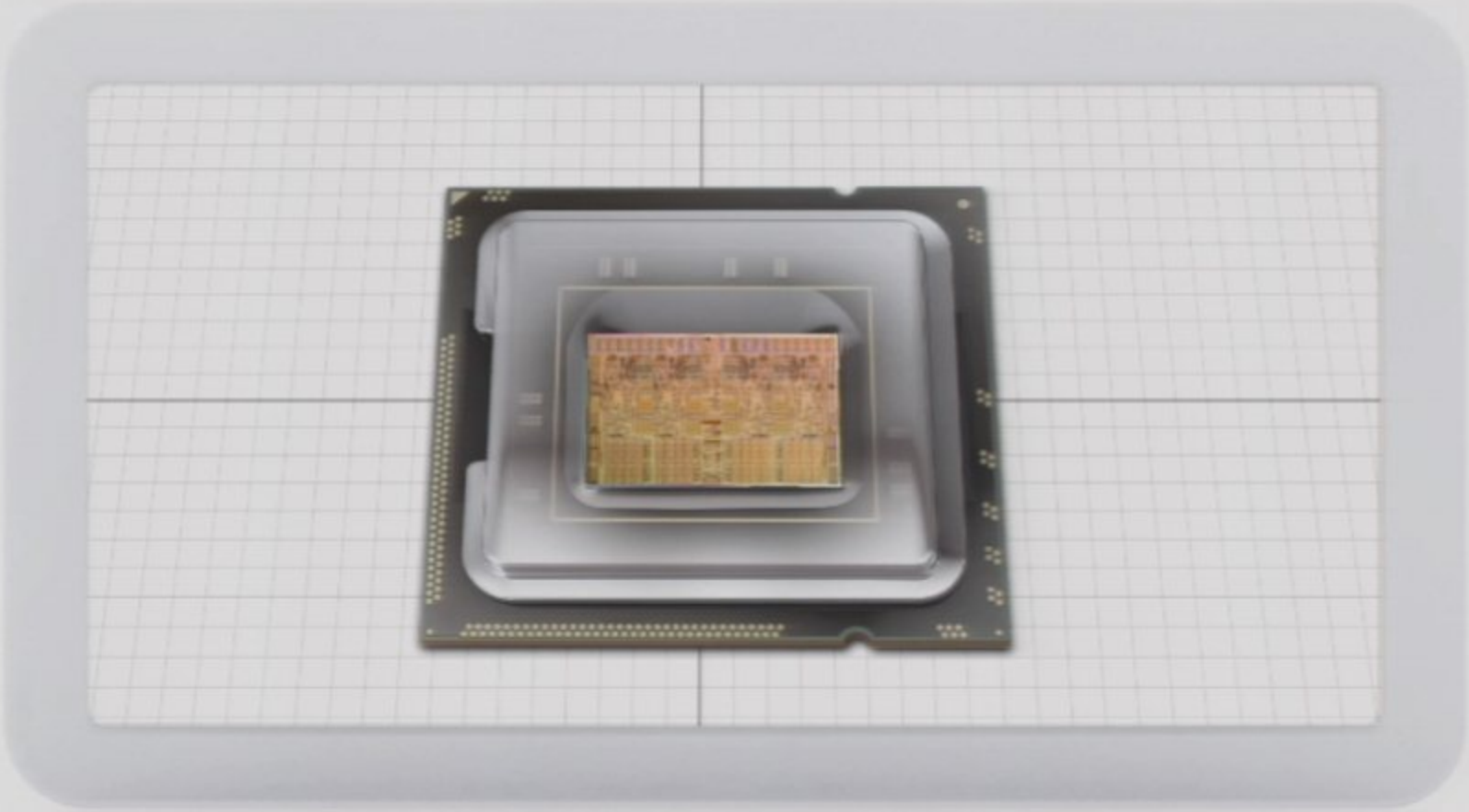
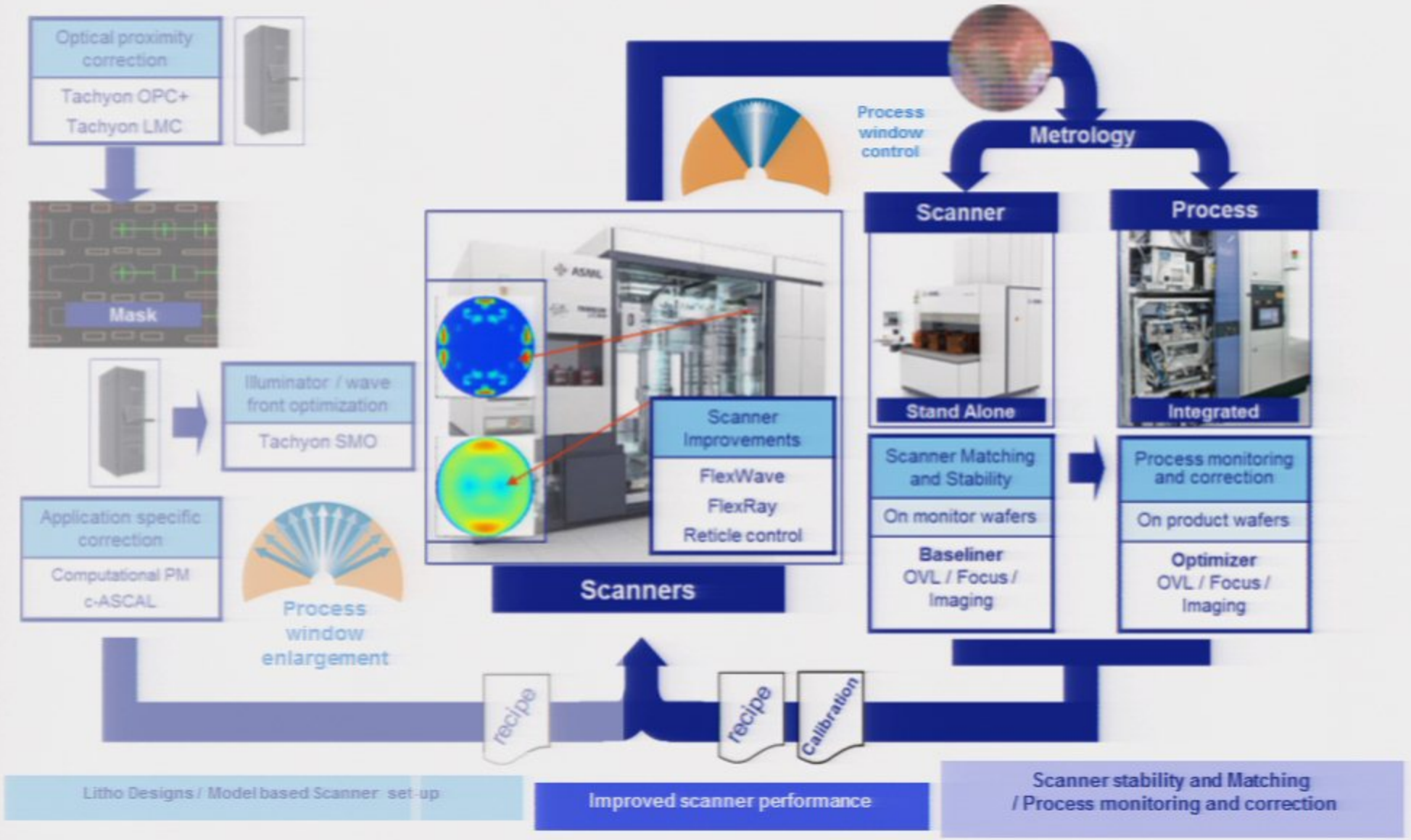


3) metrology and feedback loops to adjust settings



3) Integrated metrology drives on-product

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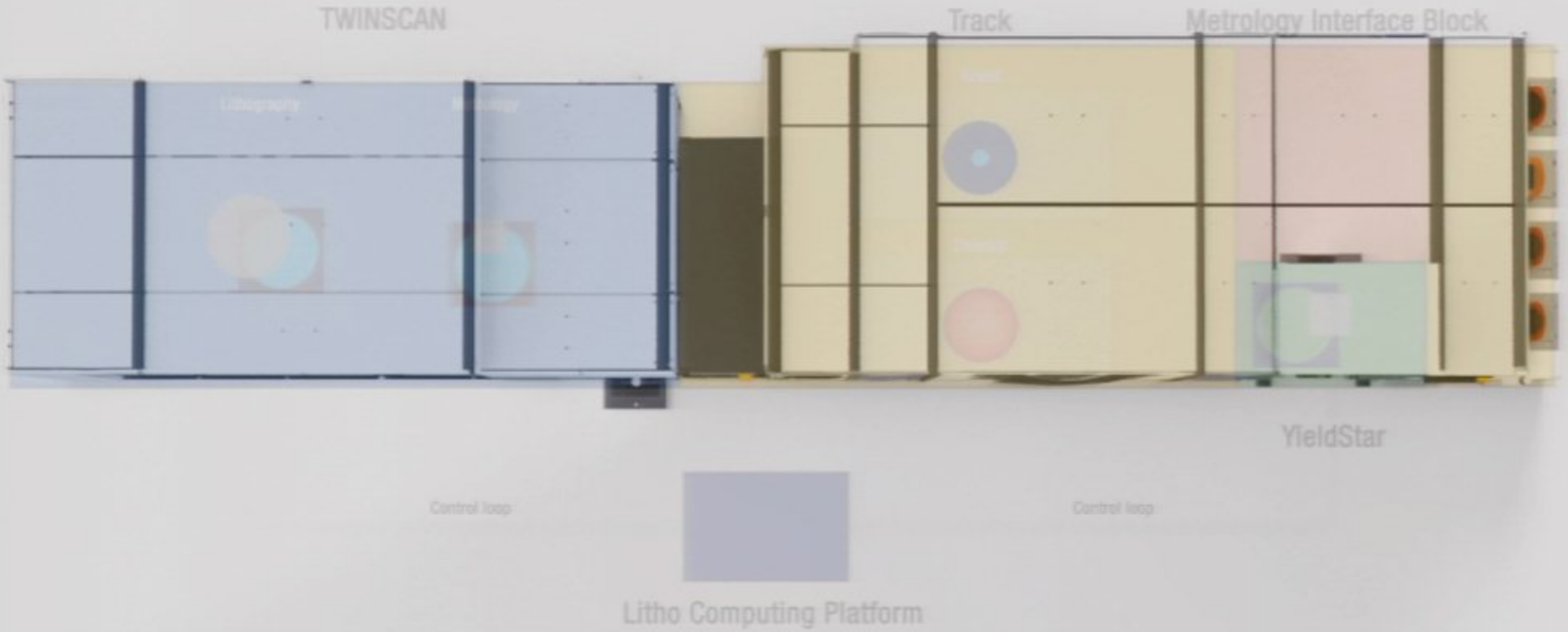

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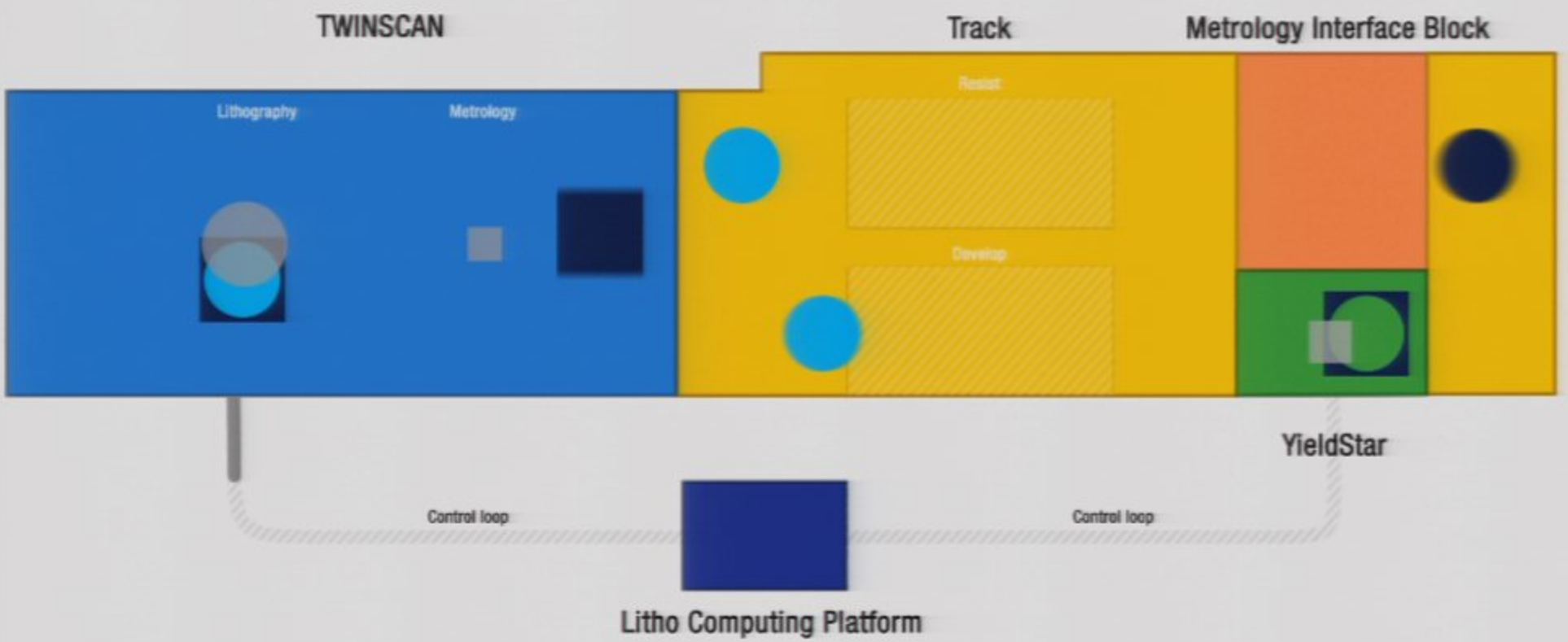

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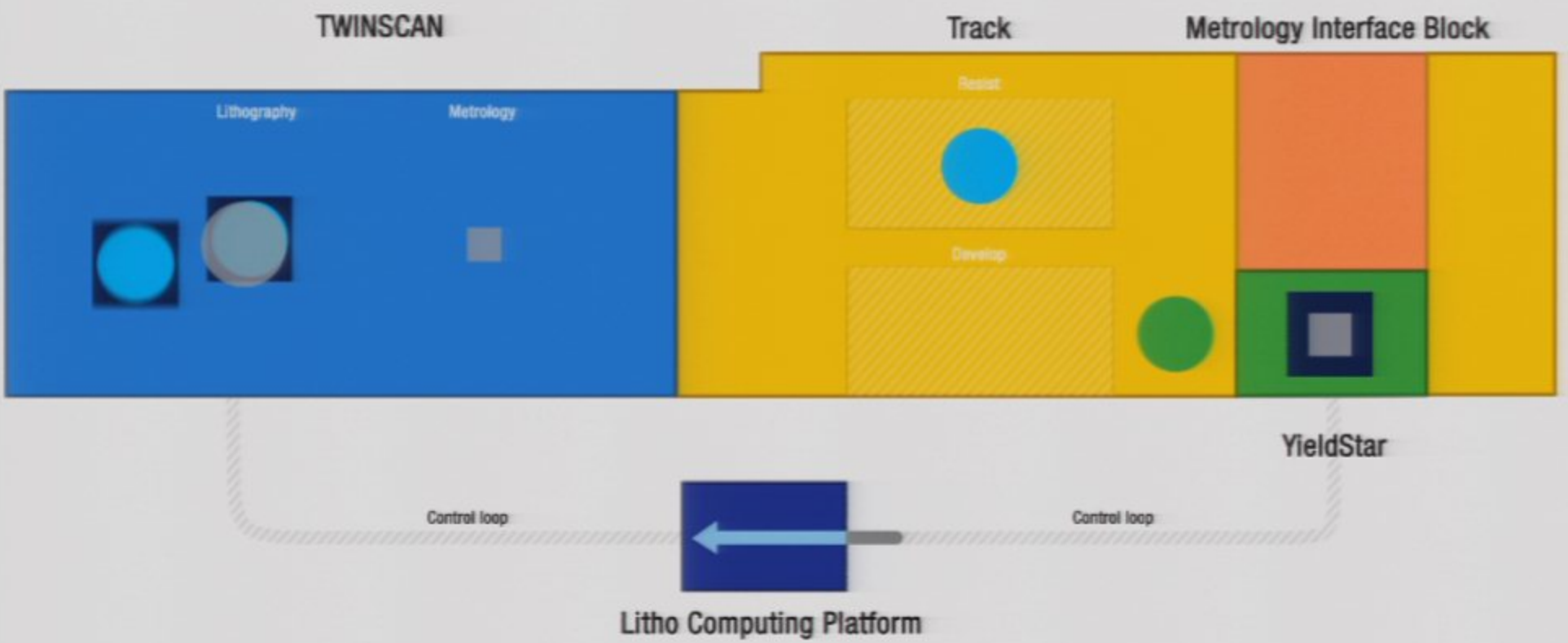

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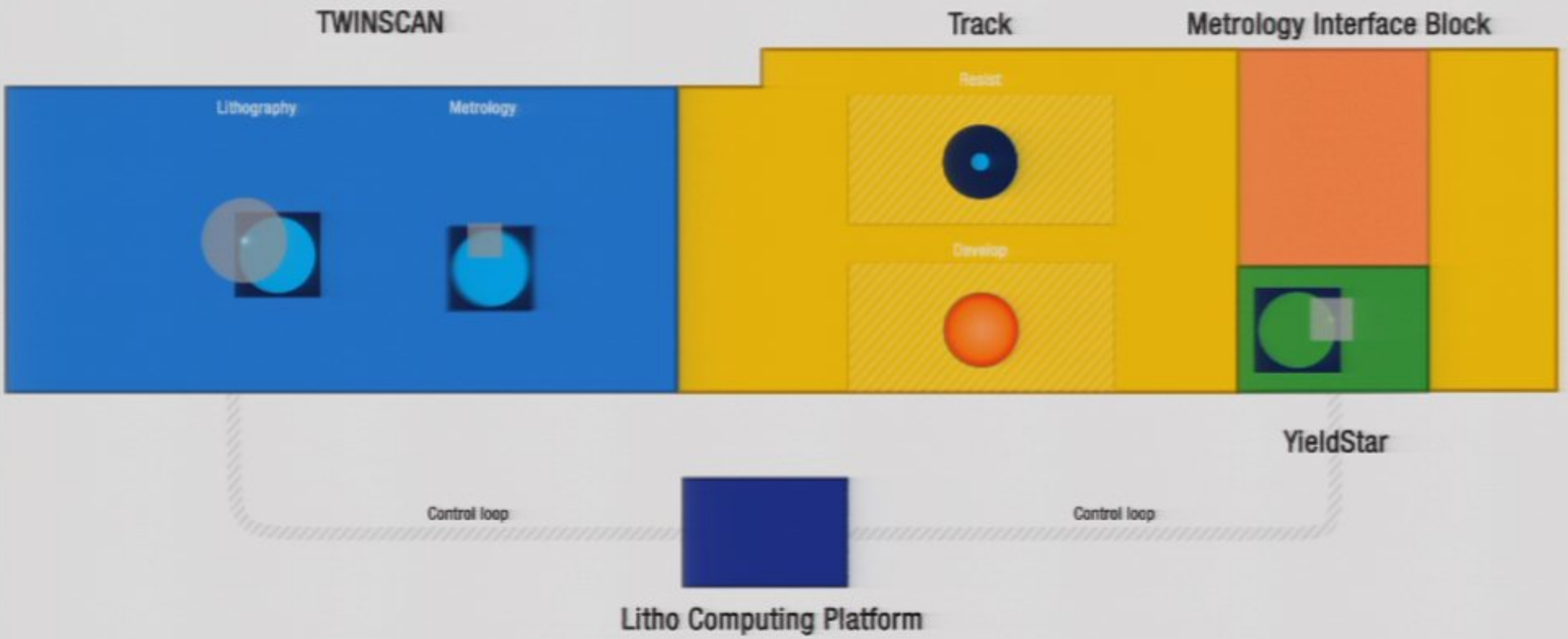

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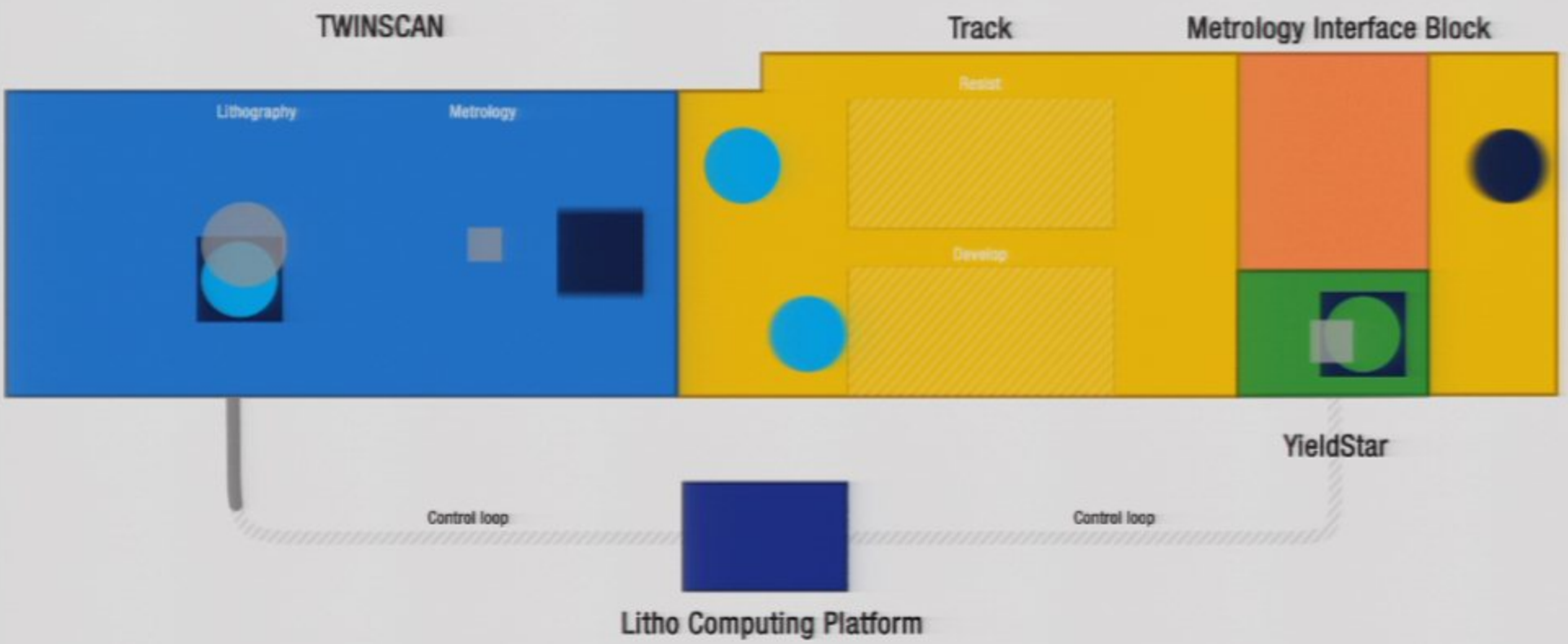

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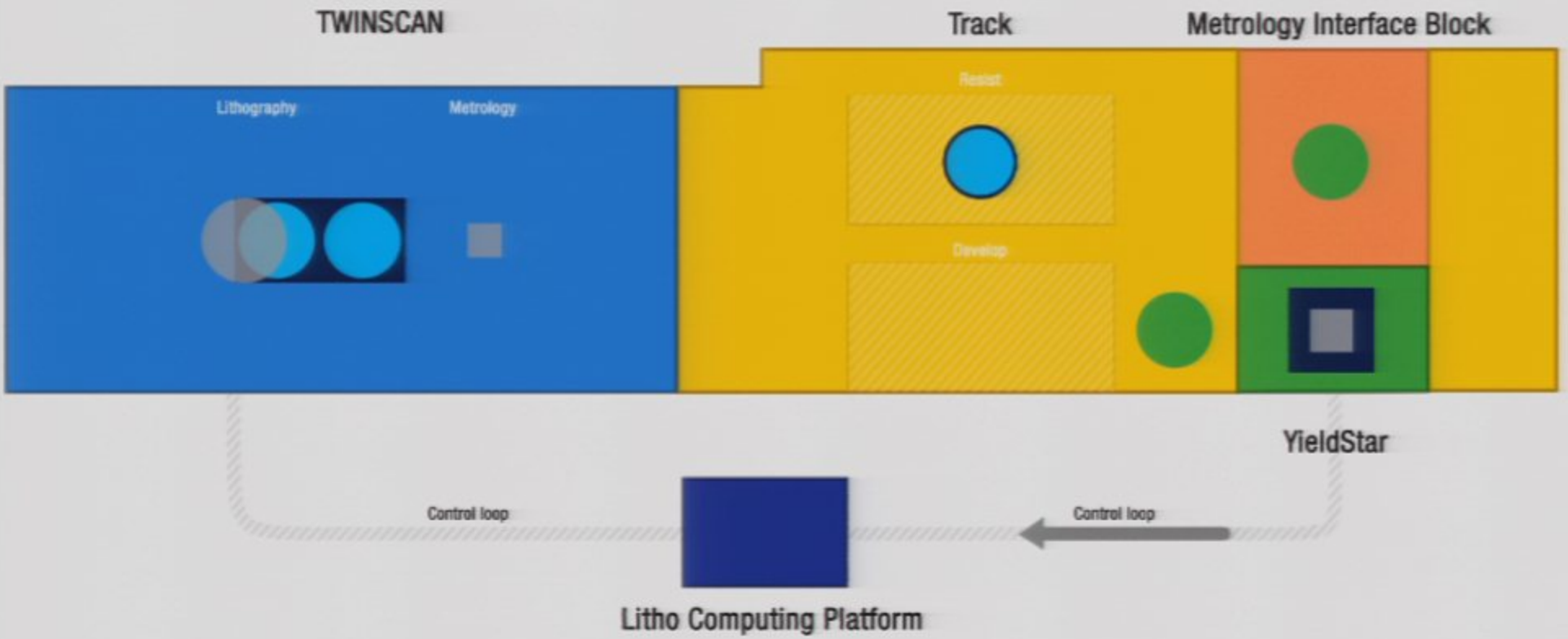

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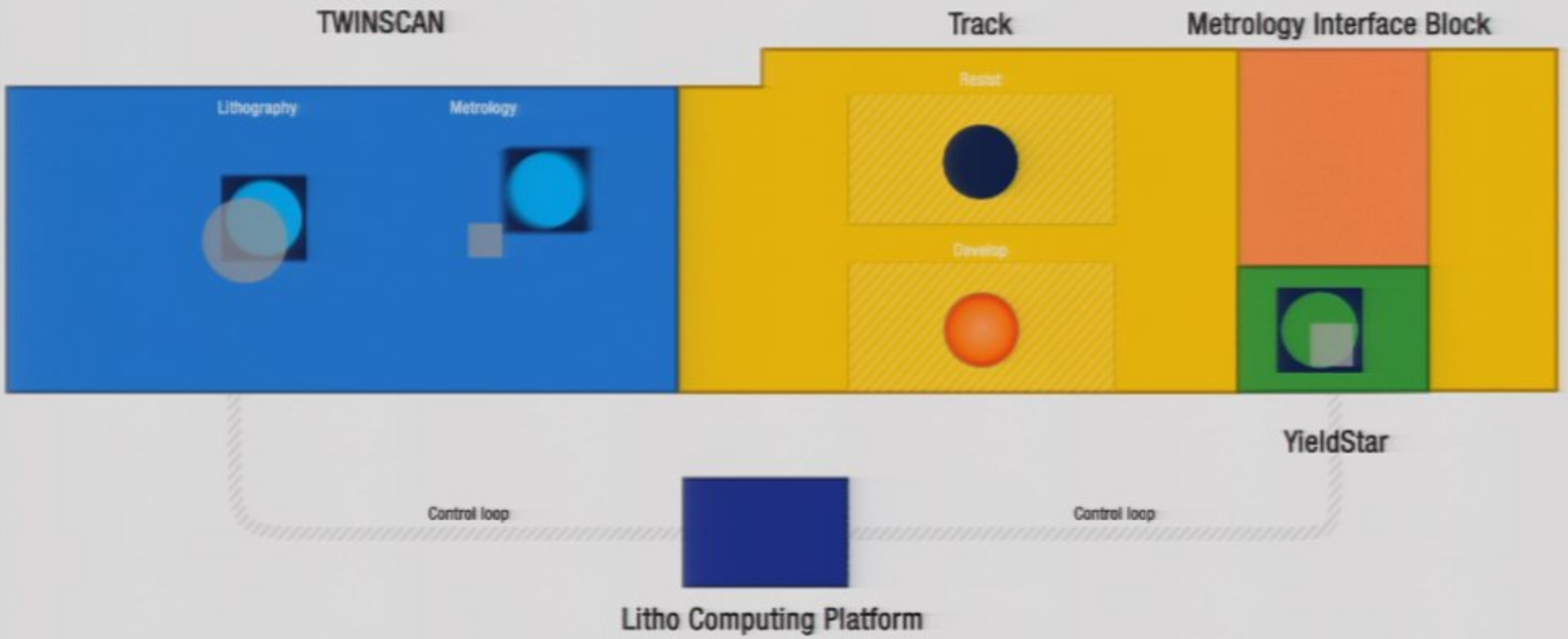
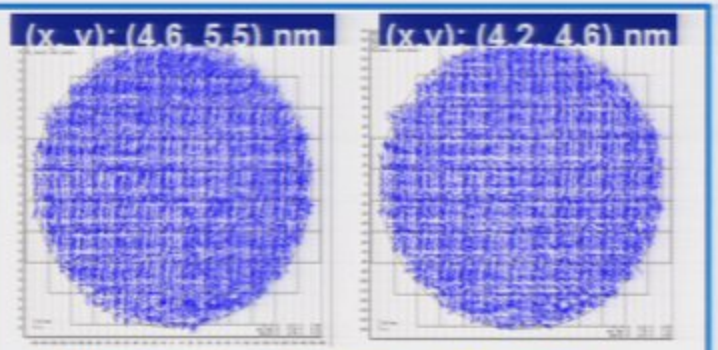


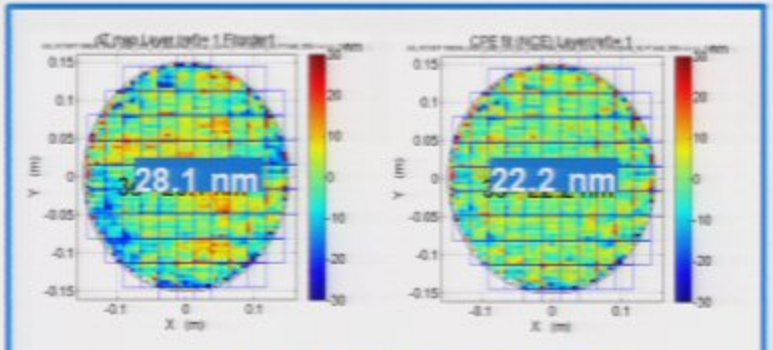
3) Integrated metrology drives on-product performance

resulting in 0.9 nm overlay and 30% focus improvement

Integrated YieldStar T200



0.9nm on-product overlay improvement measured



30 % focus uniformity improvement

Holistic lithography on immersion platform

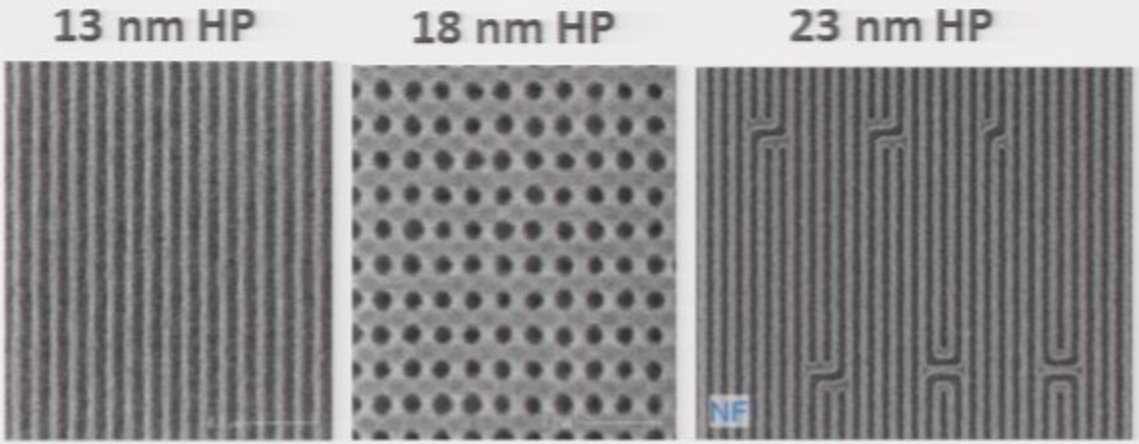
- On-product overlay budget needs to be cut from today's 8.5 nm to 3 nm in the next 4 years driven by multiple patterning.
- An holistic approach is being implemented to reach these aggressive litho targets through improved 1) machine performance, 2) process window enlargements and 3) process control.
- Productivity up to 250 wafers per hour with < 3.5 nm machine overlay will be introduced this year with improved focus control, better immersion lens, improved sensors and new wafer stage enabling high performance and cost effective double patterning.
- Source Mask Optimization and other applications are available to increase process windows.
- Affordable integrated on-product overlay measurements using scatterometry in combination with system overlay improvements are available to reach these overlay targets.

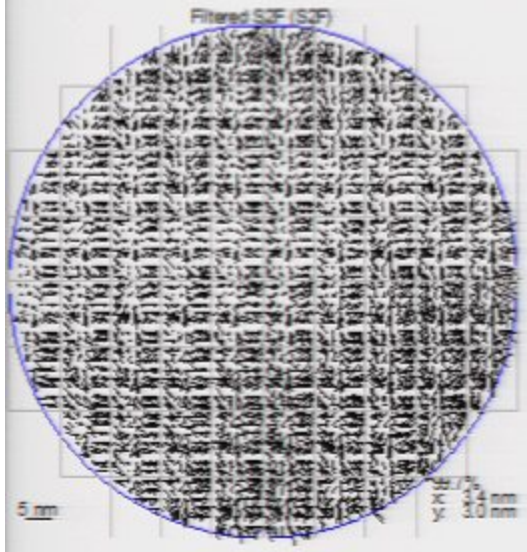
Agenda

- Shrink roadmap
- Holistic Lithography on immersion platform
- **EUV lithography**
- 450 mm
- Future

EUV litho performance qualified on 3rd generation system

Imaging down to 13 nm and EUV to immersion overlay <3.5 nm

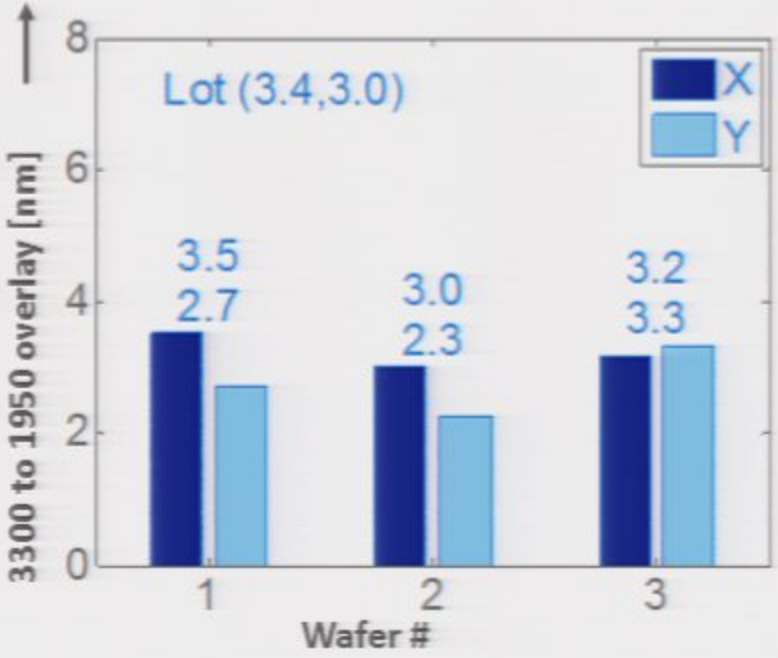




Full wafer

Matched machine overlay

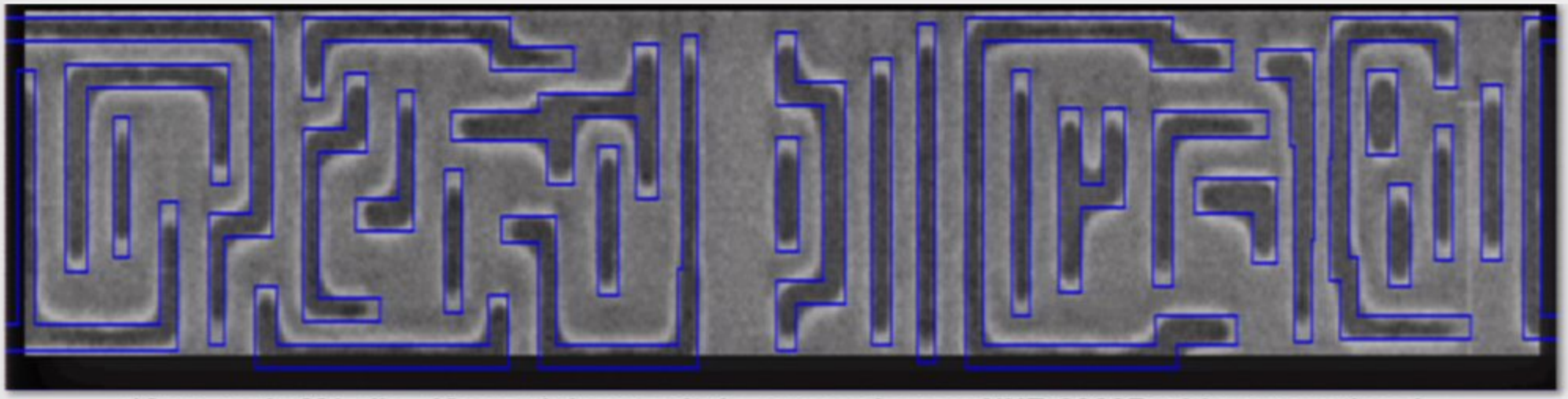
NXE:3300B (EUV)
to
NXT:1950 (ArFi)



Using 13 nm wavelength with reflective 0. 33 NA optics

NA – Numerical Aperture
HP – Half pitch

0.33 NA EUV enables single exposure 10 nm node



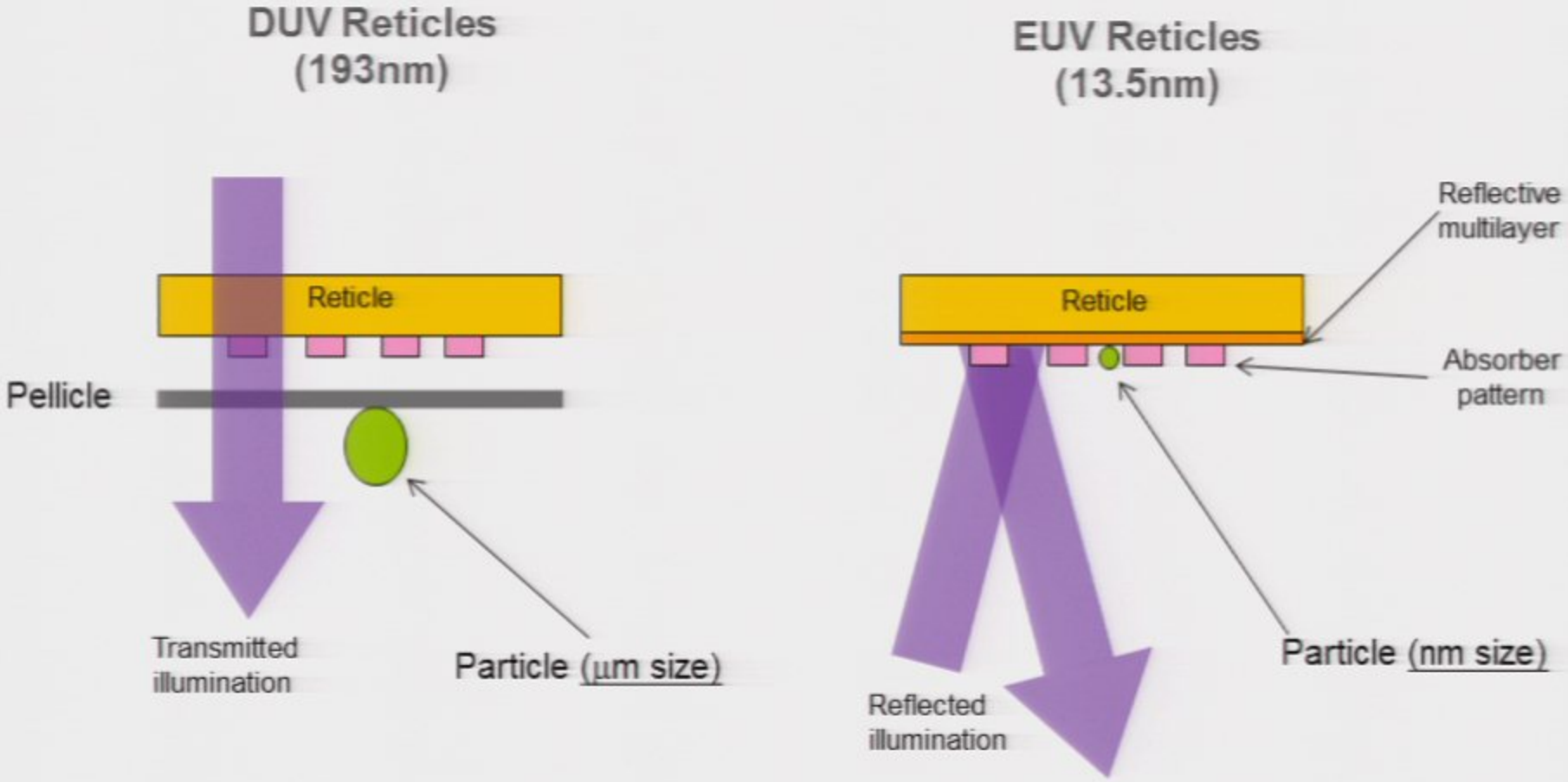
10nm node M1 clip, 46nm minimum pitch, exposed on an NXE:3300B with conventional illumination. Clip courtesy of ST

EUV	ArFi
Single exposure shows good resemblance between reticle and wafer layout	Can only be done with double patterning (LELE)
Best HV focus difference <10nm	Best HV focus difference up to 60nm
Measured UDoF of 100nm	Typical UDoF ≈ 50nm

UDoF – Usable Depth of Focus LELE – Litho Etch Litho Etch

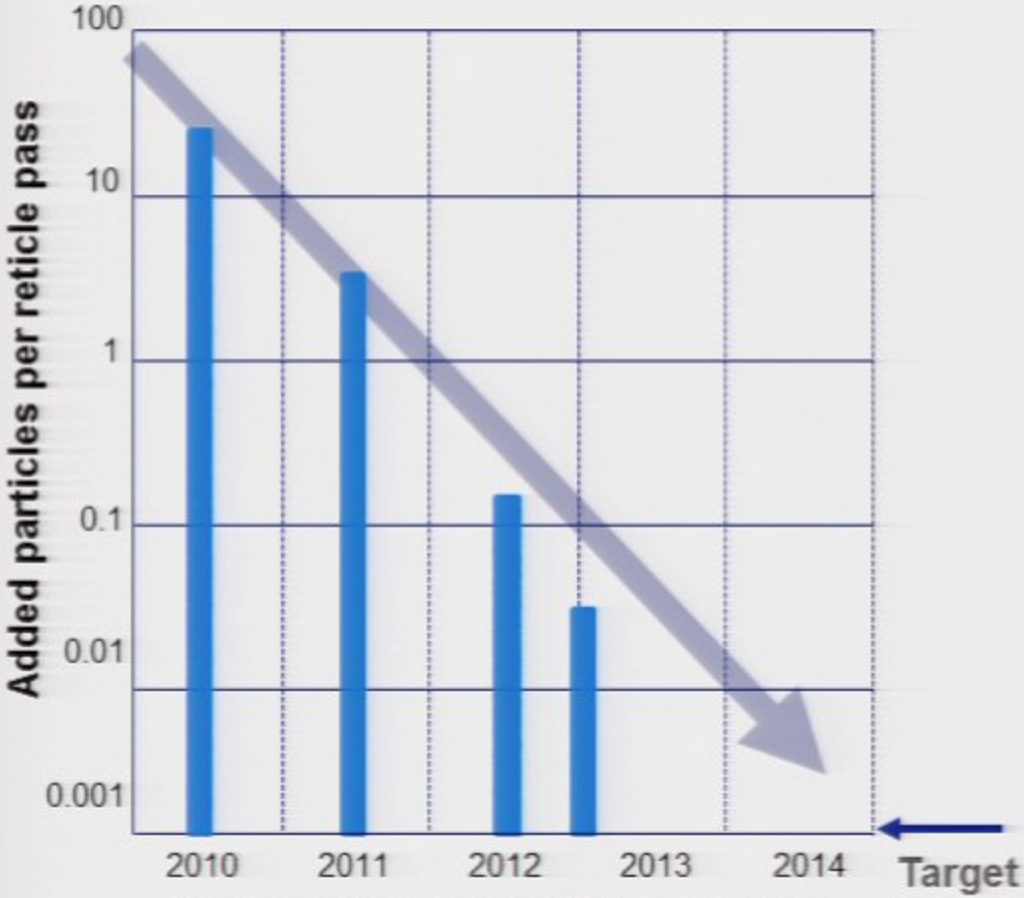
The mask defect challenge

Challenging defect requirements on reflective pellicle less EUV mask



The mask defect challenge

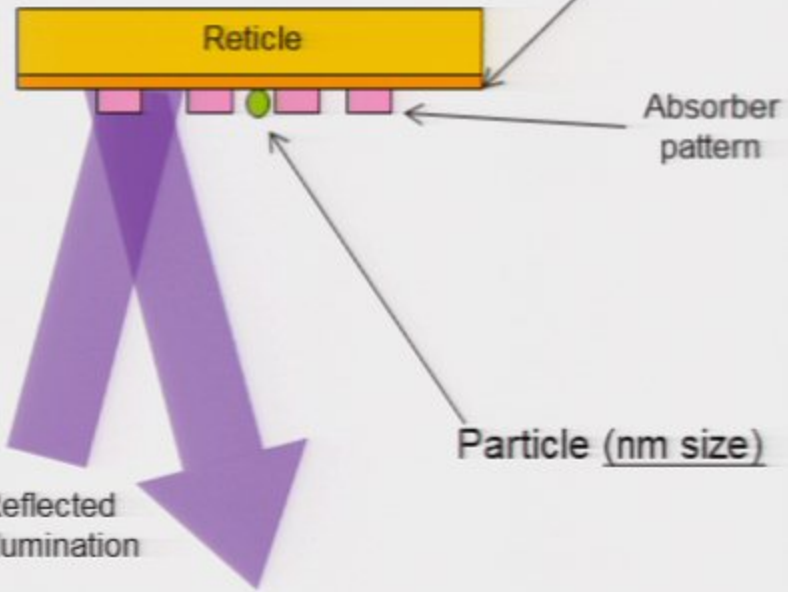
Substantial progress made toward defect free mask handling, pellicle would reduce defect requirements substantially



Progress made on ASML machines on added particles per reticle exchange over the past few years

Target performance for full production **without** pellicle

EUV Reticles (13.5nm)



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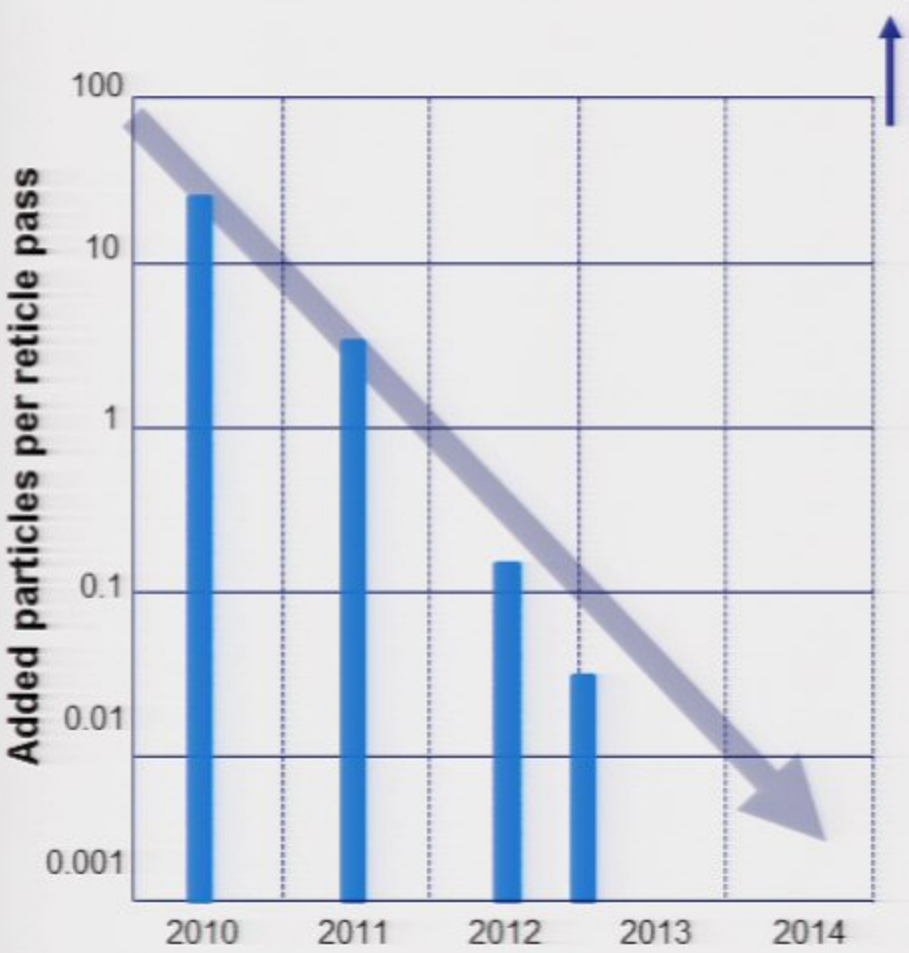

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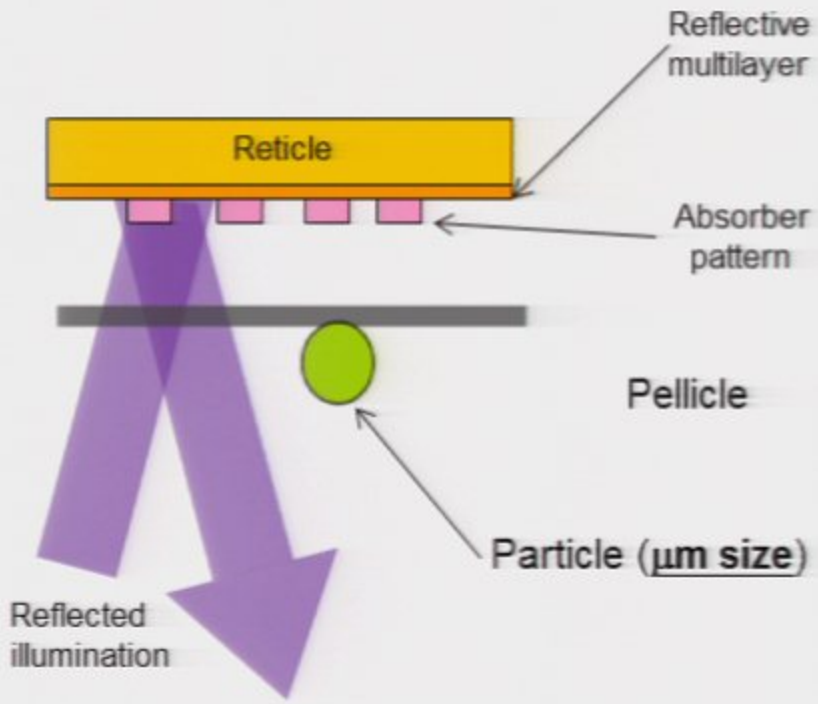
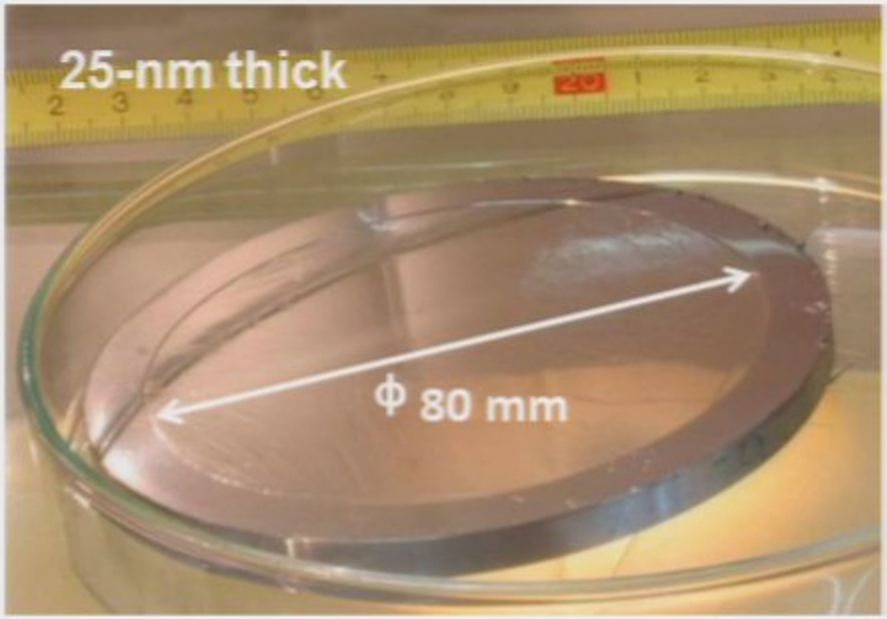
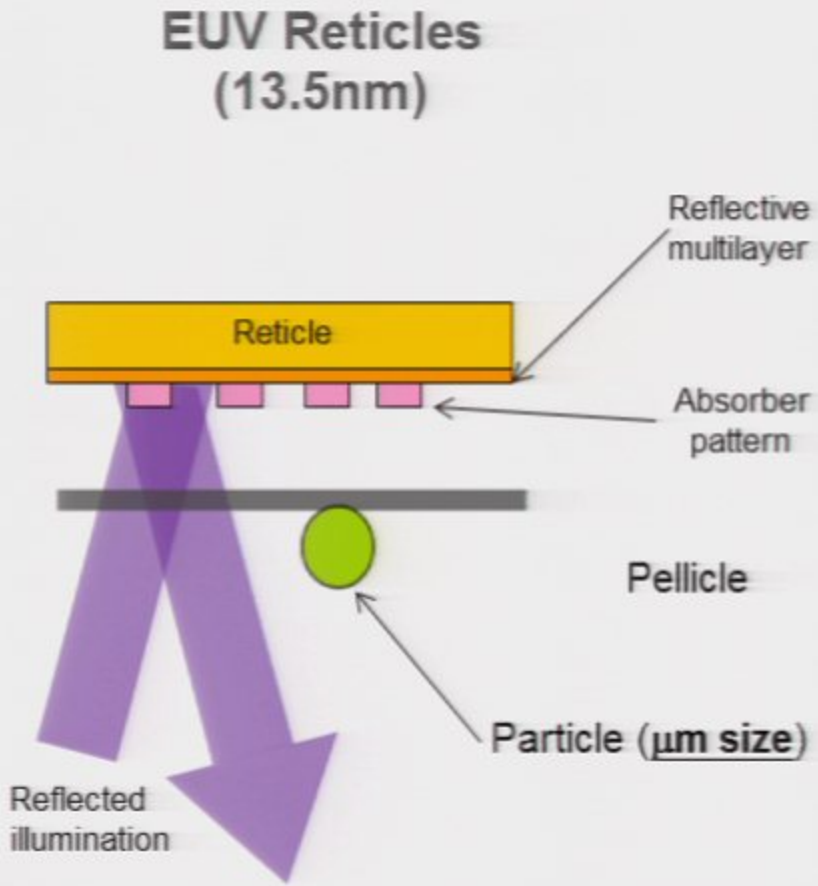


The mask defect challenge

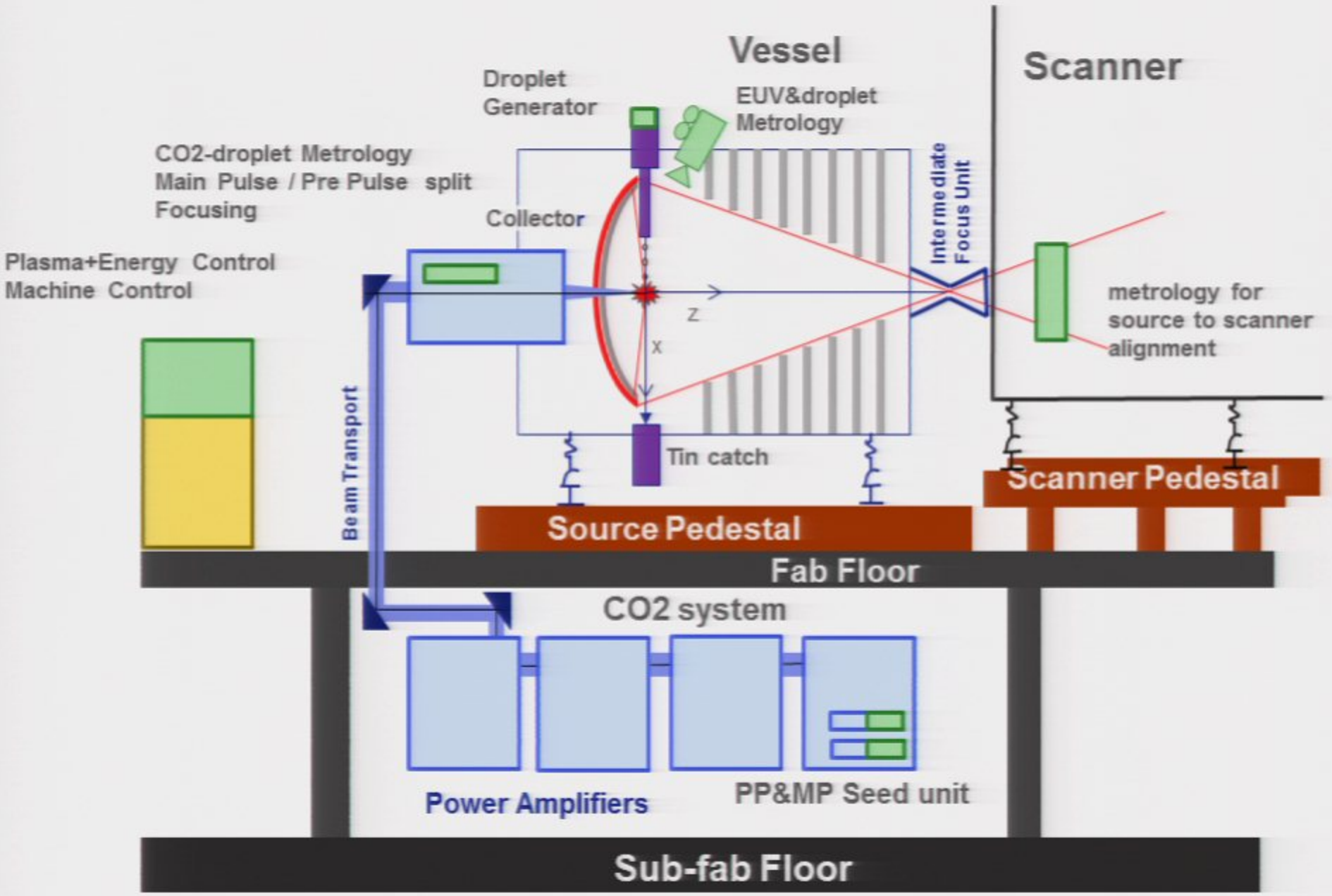
EUV pellicle considered as backup with minimum transmission and imaging loss





- Requirement: 90% transmission, 114x142 mm²
- Status: 83% transmission, Φ 80 mm

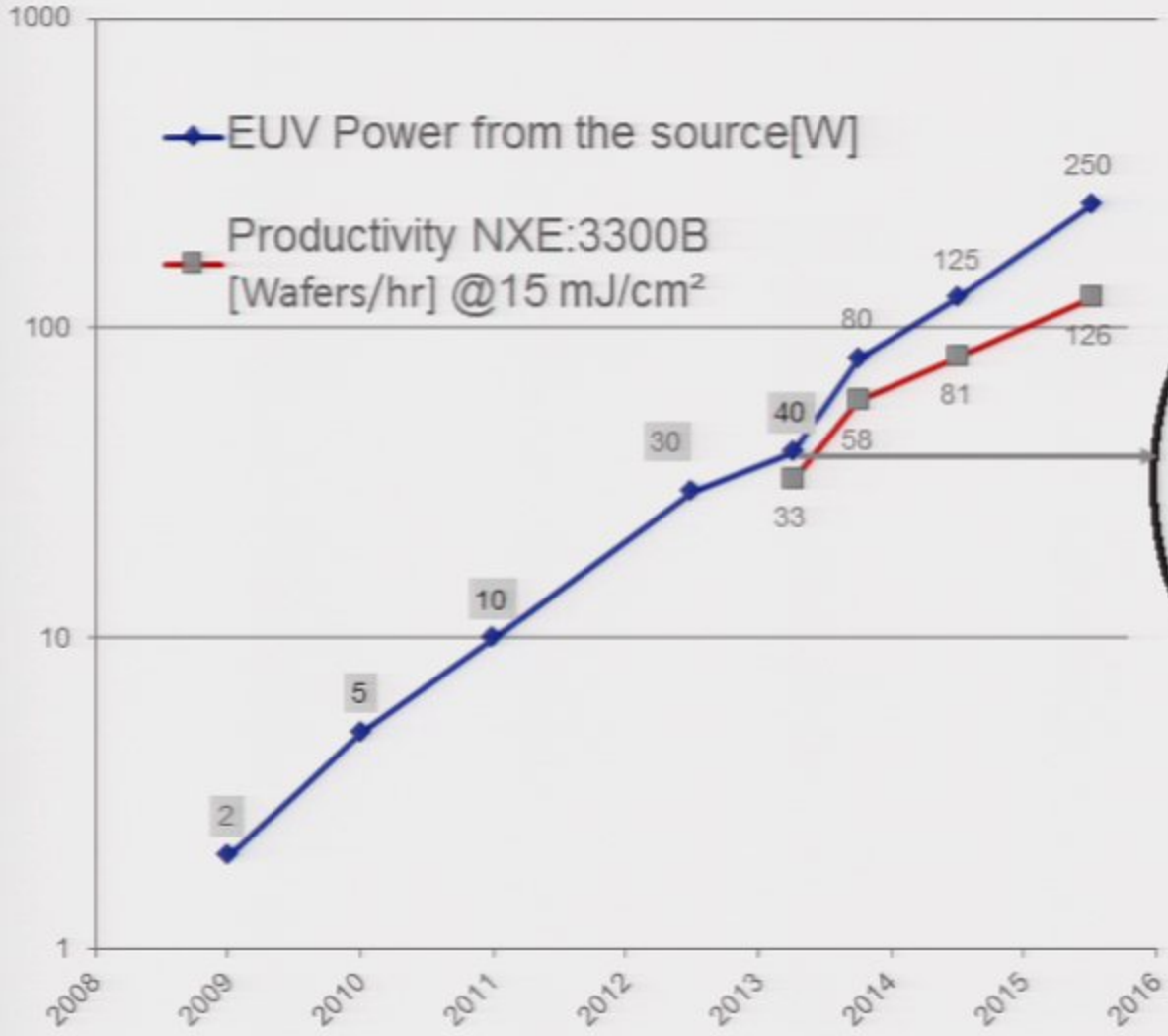
EUV source system cross-section

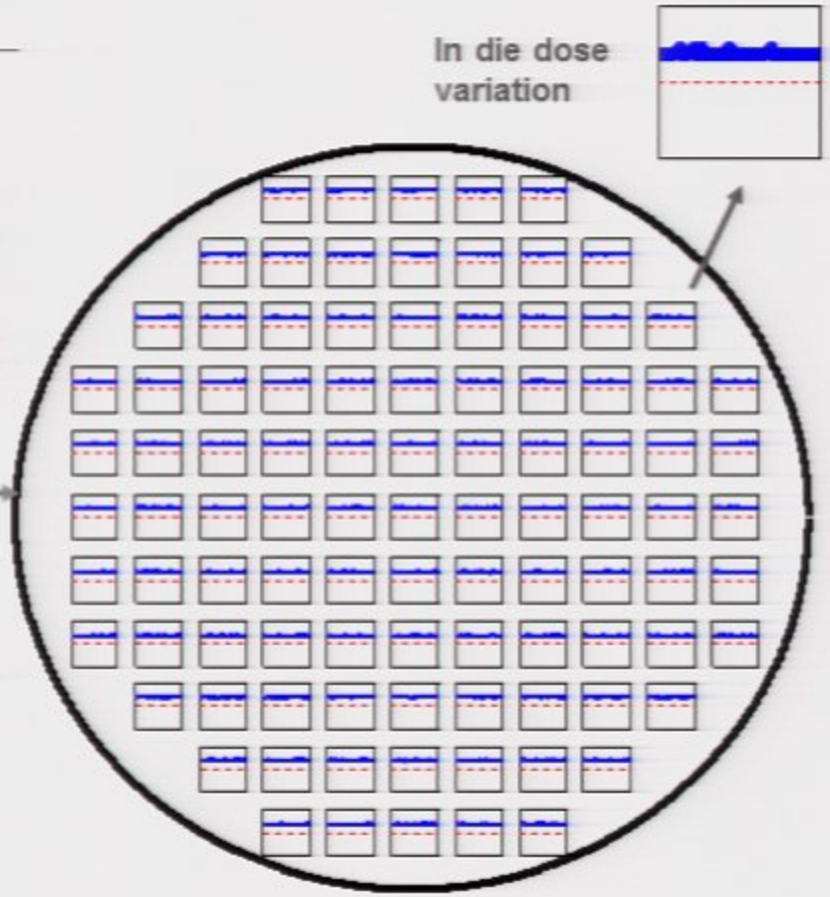


x = droplet stream direction, z=CO2 light direction, y=orthogonal

EUV Source Power Progress

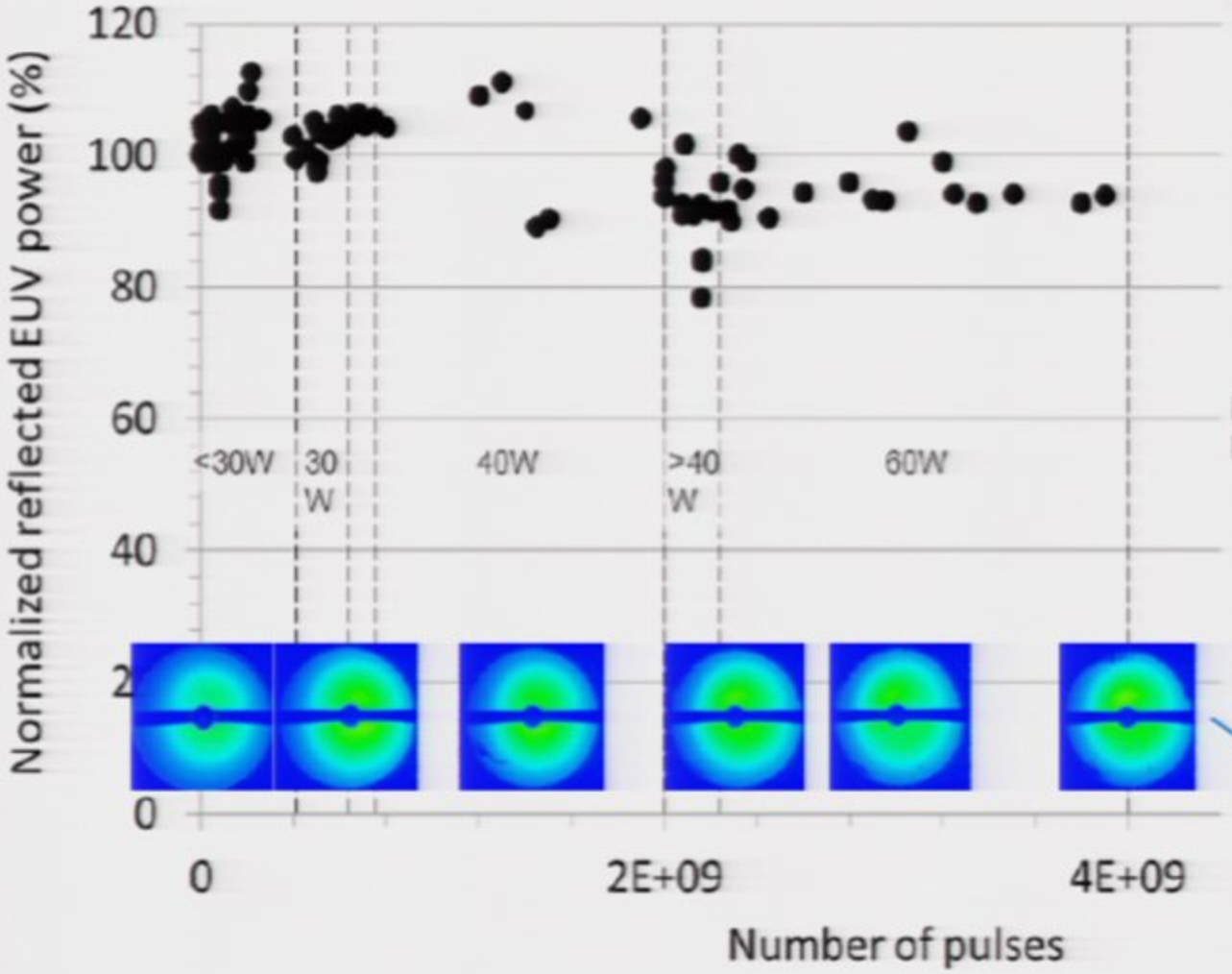
incl. throughput estimates for NXE:3300B EUV system



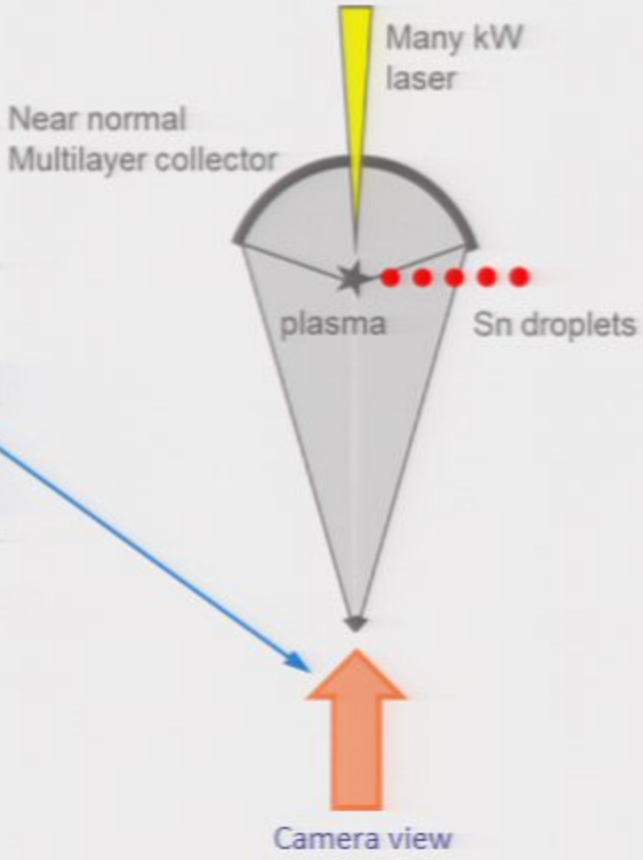


At 40 W: Simulated die yield 99.99% at 0.2% dose, over 5 consecutive runs of > 1 hr representing > 165 exposed wafers @ 15 mJ/cm²

EUV collector reflection stability up to 60 W

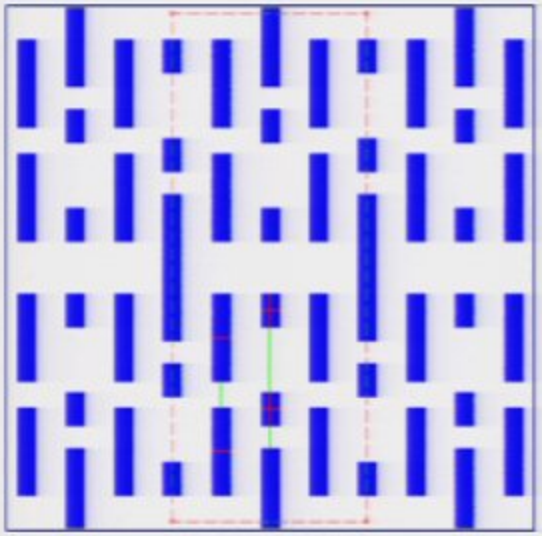


4 B pulses represent ~40 hr continuous exposures.



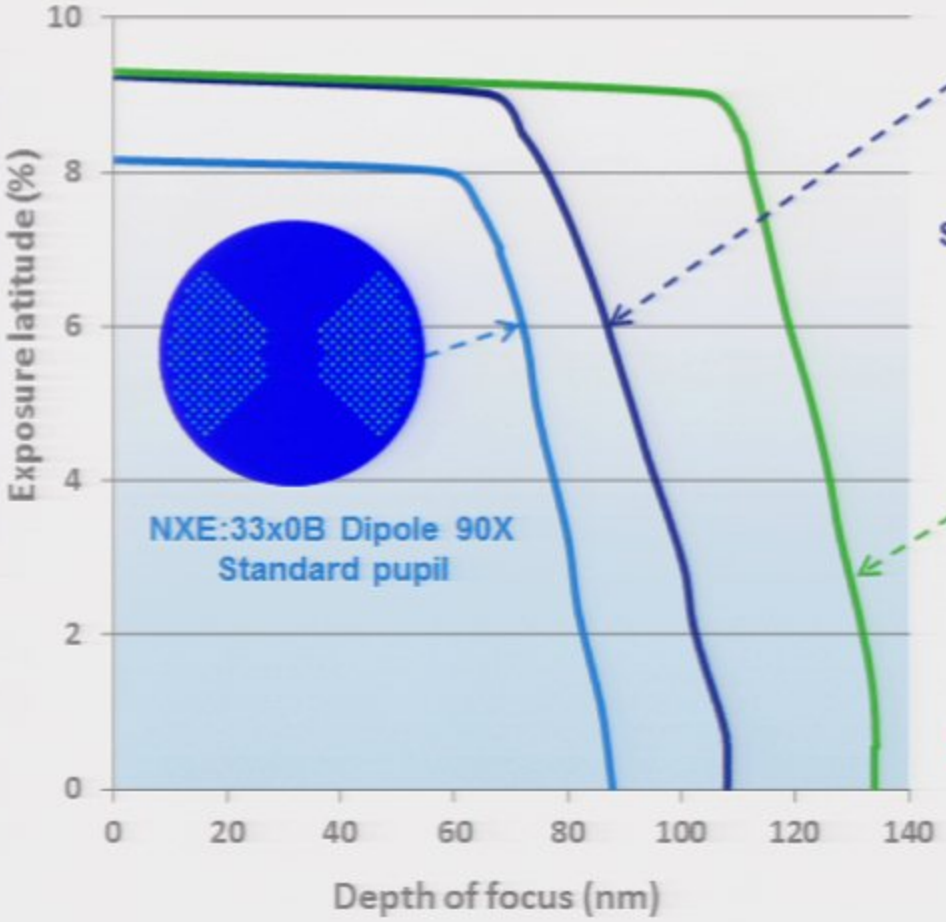
EUV extendable to 7 nm node through holistic approach

Source mask optimization at 0.33 NA and reducing the pupil filling to 20% maintaining full productivity



Logic 7 nm node

- Local interconnect layer
- Bright field
- Feature width = 12 nm
- Feature pitch = 32 nm



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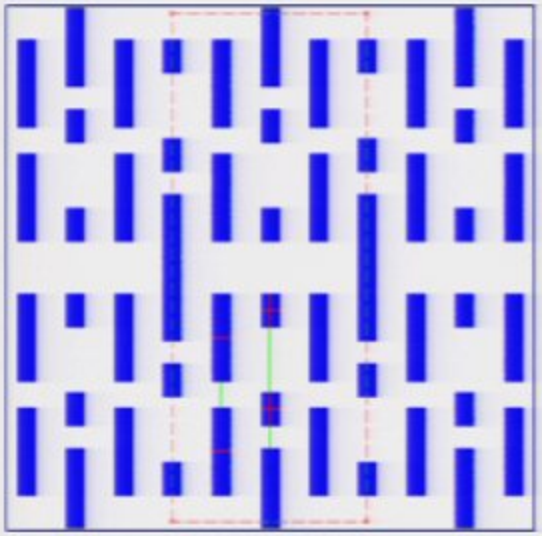

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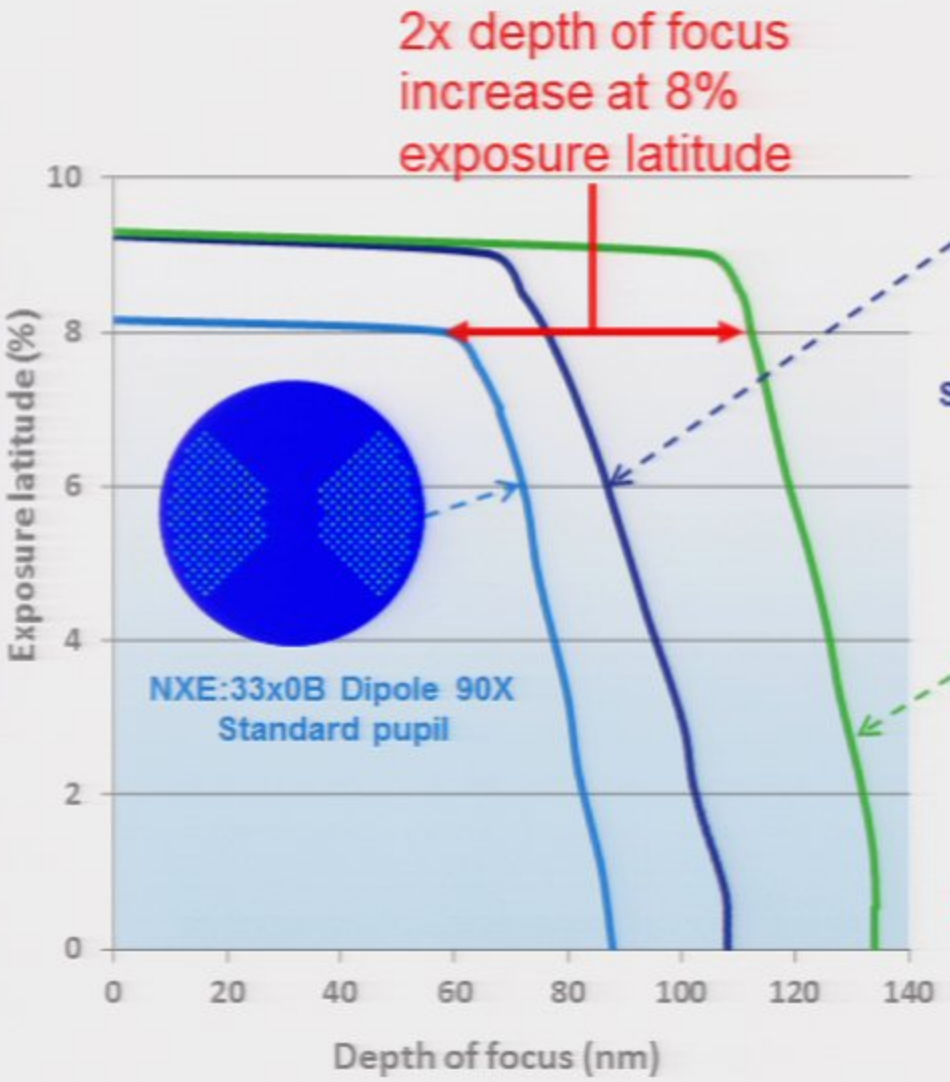


Preparing EUV for device production

- EUV litho performance meets customer expectations except operational economics (productivity and uptime). Shipment of the 3rd generation EUV tools to multiple chipmakers, NXE:3300B, starting mid 2013.
- ASML and Cymer[1] boost effort to secure the commitment to customers for 2014 delivery of 70 Wafers per hour @ 15 mJ/cm².
- Future extension of the current 0.33 NA technology is planned through system improvements – overlay, projection lens, illuminator, resist – to 7 nm half pitch using double patterning.
- ASML has agreed an EUV funding program up to EUR 828 million over the next 5 years with its customers Intel, Samsung and TSMC.

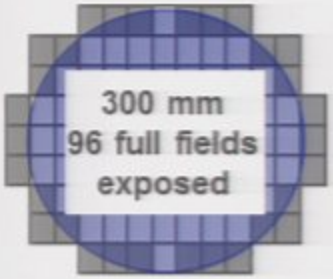
[1] Note ASML and Cymer announced their intention to merge in Oct. 2012

Agenda

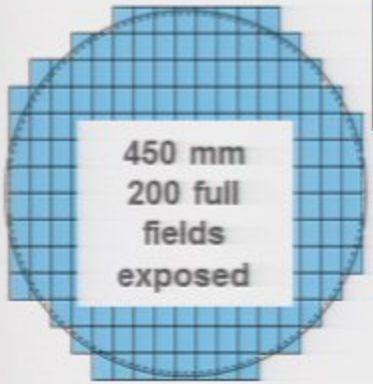
- Shrink roadmap
- Holistic Lithography on immersion platform
- EUV lithography
- **450 mm**
- Future

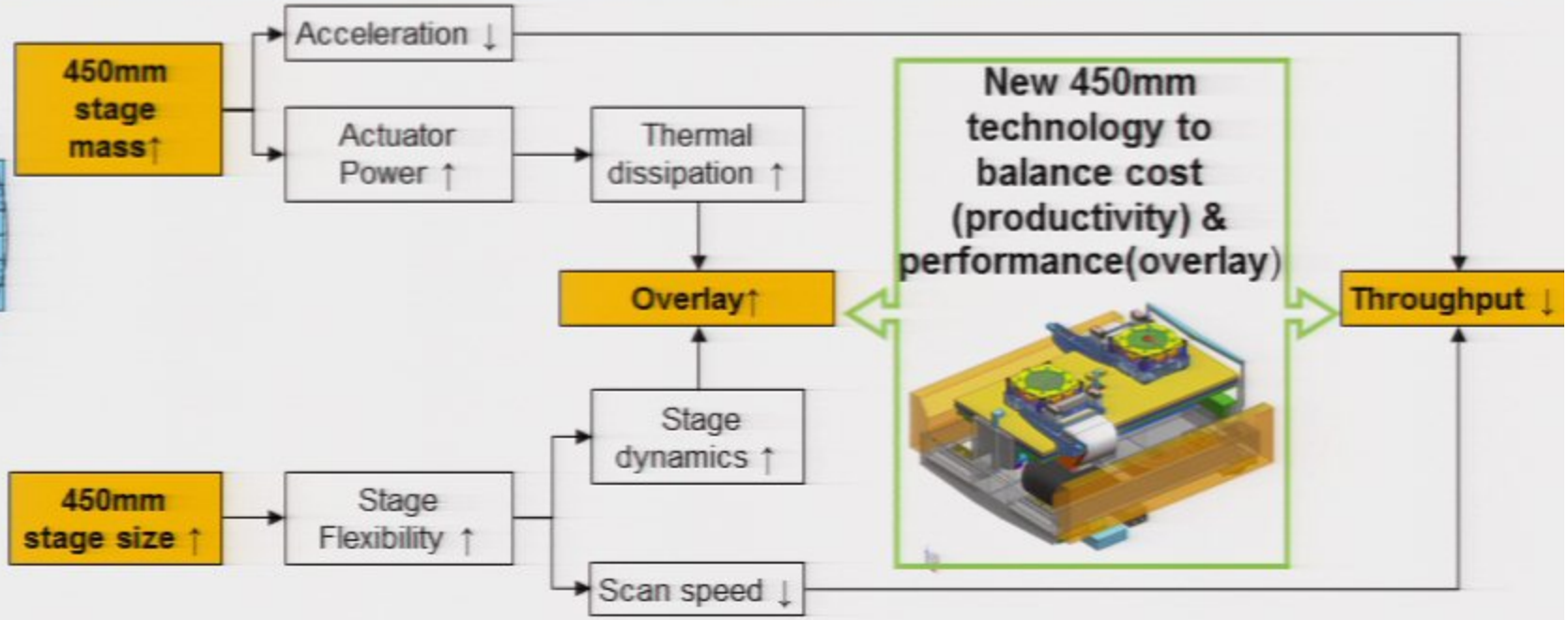
Litho economics 300 mm ➔ 450 mm challenging

New technology needed to stay neutral in cost



	throughput			Relative cost	
	Wafers per hour	m² Si/ hour	450mm/ 300mm	Cost	Cost/ m² Si
300 mm limit	250	18	1.0	1.0	100%
450 mm linear stage scaling	100	16	0.9	1.1	122%
450mm new technology	125	20	1.1	1.1	100%





450 mm QXE: extension 300 mm NXE EUV system

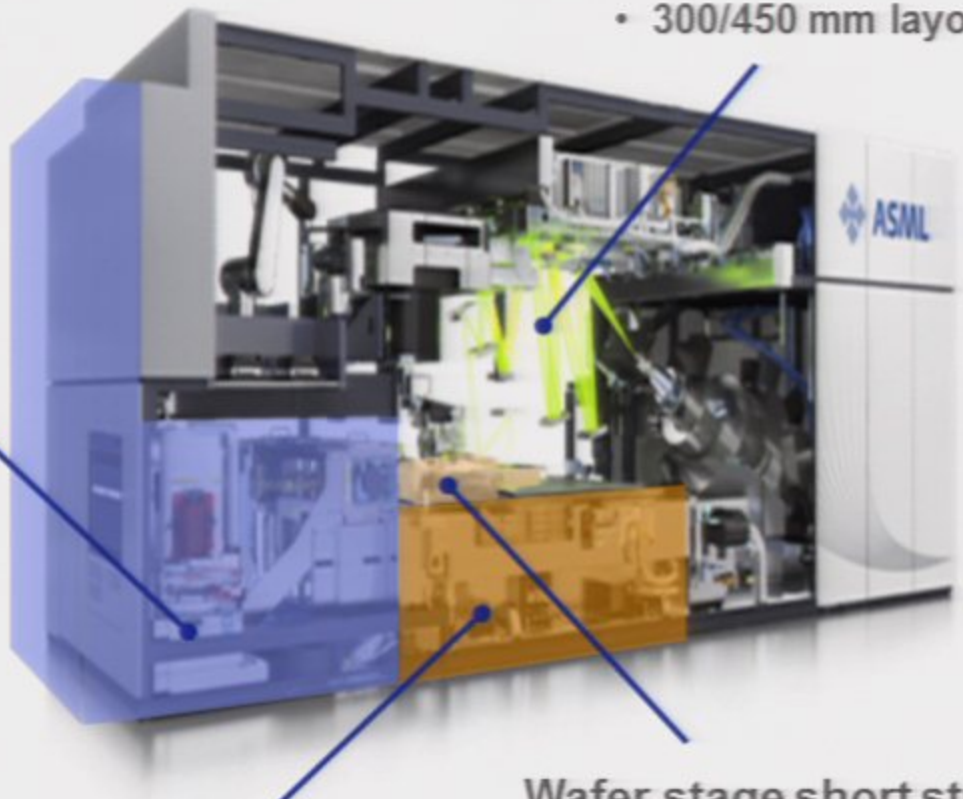
EUV 450 mm systems operational at customers in 2015

Wafer handler

- Improved thermal control
- <0.7 m longer
- 450mm atmospheric handler
- 450mm load locks
- 450mm wafer exchanger

Metroframe

- 300/450 mm layout for interferometry



Modified wafer stage base module

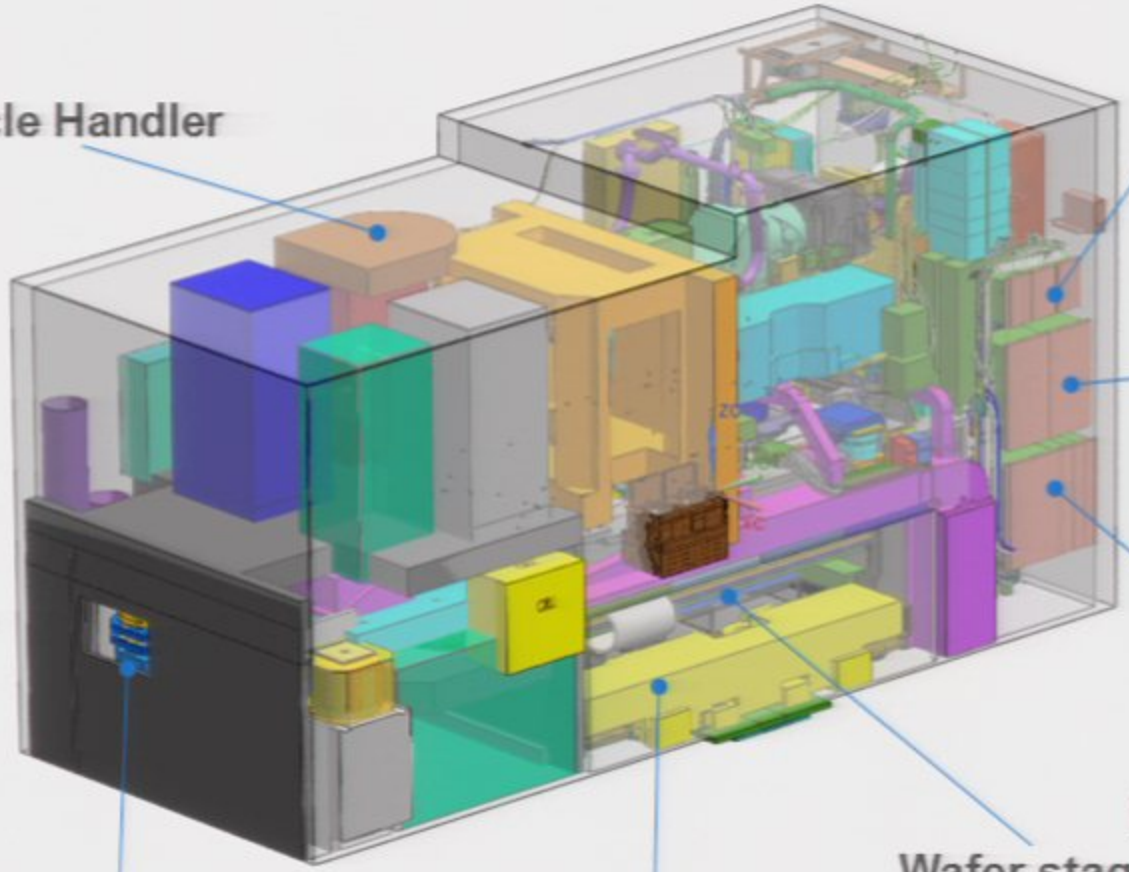
- Additional facilities for wafer clamp (pressure pulse compensators, etc)

Wafer stage short stroke

- Improved servo control
- Improved stability
- 450mm wafer clamps with improved thermal control

450 mm QXT immersion: almost completely new body

Immersion 450 mm systems operational at customers in 2016 with footprint equivalent to EUV; platform supports dry systems



450 mm for productivity and cost

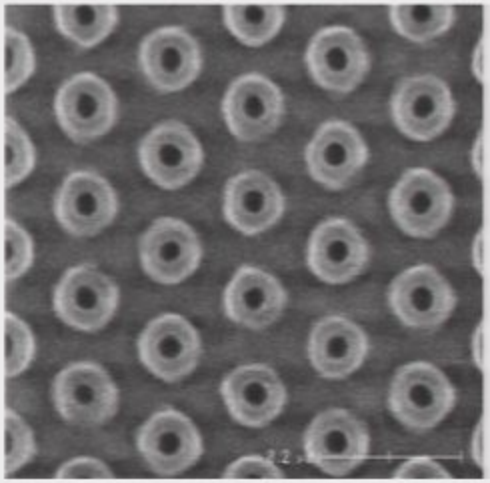
- Shrink becomes a bigger risk for our customers given the overall technology risk. 450 mm looks like a doable cost reduction scenario. However the litho-specific cost reduction on 450 mm will be limited, given its productivity scales fundamentally negatively with the wafer surface area.
- ASML is engaged with a 450 mm funding program up to EUR 553 million over the next 5 years with customer Intel for 2015-2016 ramp-up.
- 450 mm litho operational as from 2015 using EUV systems and 2016 for immersion systems
- Above will support 450 mm wafer production starting 2018
- Overall concerns remain of too limited overall industry 450 mm implementation plans

Agenda

- Shrink roadmap
- Holistic Lithography on immersion platform
- EUV lithography
- 450 mm
- **Future**

Future lithographic trends

- EUV will likely be scalable to sub-5 nm half pitch using a combination of higher apertures, double patterning and possibly lower wavelengths
- Alternative lithography techniques will give the resolution, however:
  - E-beam productivity fundamentally drops steeply as function of resolution
  - Imprint yield is hampered by defects
- Directed self assembly, if applied, will be complementary to EUV and can be used as a more cost-effective alternative to current double patterning and/or improve CD uniformity.

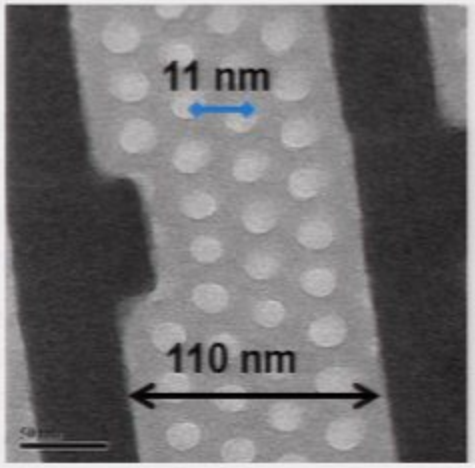


Contact hole healing

CD 79 nm -> 29 nm
CDU: 3.5nm -> 1.3 nm
CHR: 2.7 nm -> 0.7 nm
Contact Placement accuracy:
X: 2.0 nm
Y: 2.1 nm

Directed Self Assembly using litho based pattern pinning

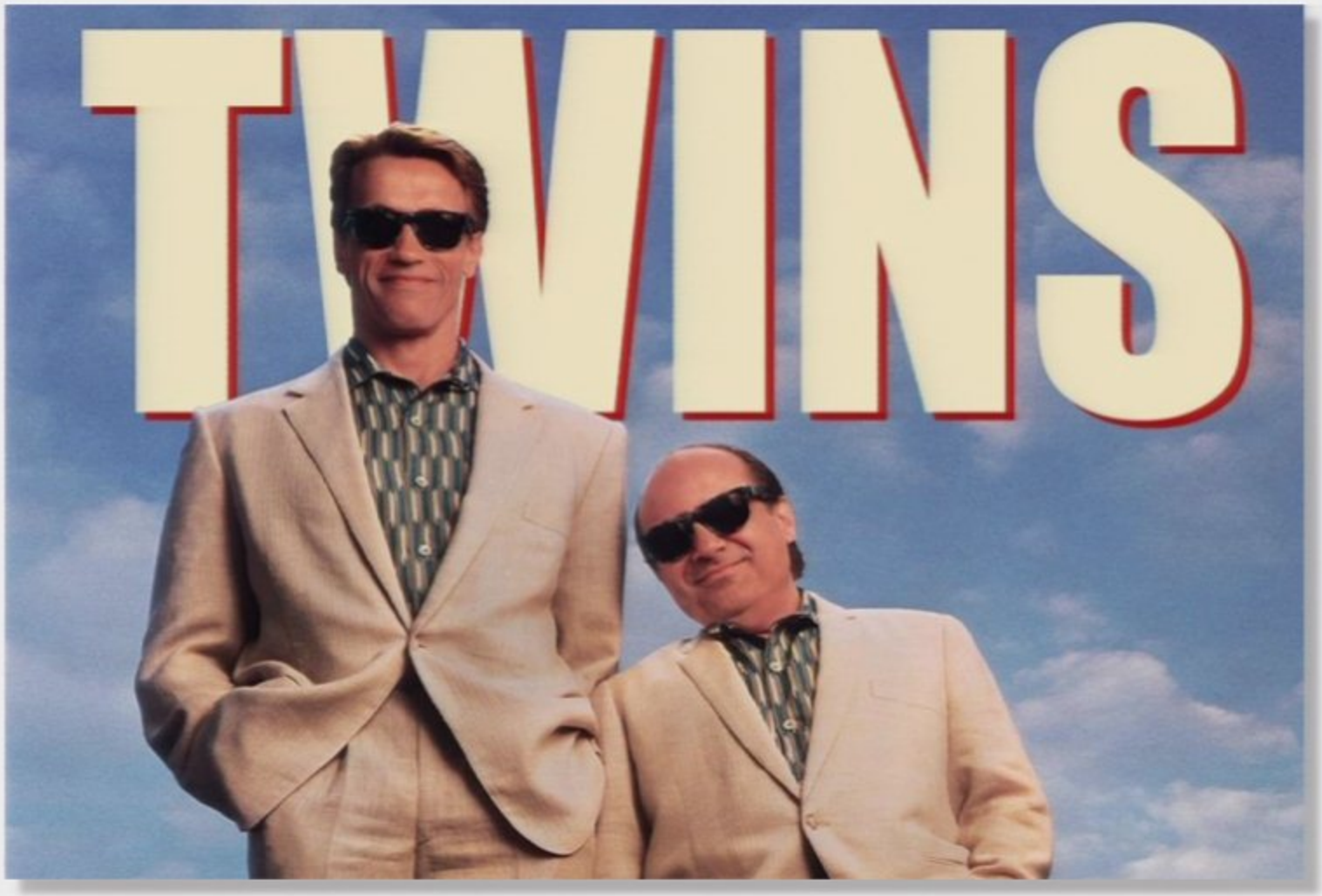
Contact Placement accuracy:
X: 3.7 nm
Y: 5.0 nm



Affordable litho scaling performance an cost achievable

- Drive productivity and yield (overlay) on immersion platform enabling double patterning
  - Down to 10nm microprocessors and NAND, 20nm DRAM
- EUV needed for unconstrained scaling and cost
  - EUV to start device production in 2014 at 0.33 NA, scalable down to 7 nm half pitch through upgradable system improvements and double patterning.
- 450mm the next cost reduction opportunity
  - Scheduled to start device production in 2018 to reduce further cost

We are much alike: you wrestle electrons, we wrestle photons

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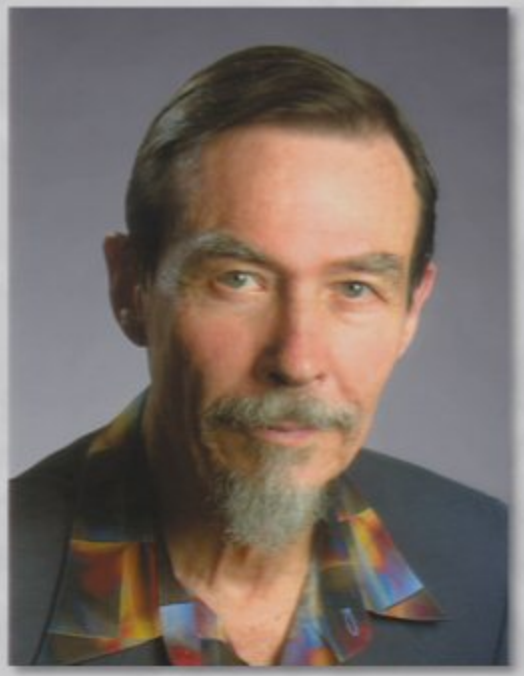

The Evolution of Technology

Carver Mead,
Professor Emeritus, Caltech,
Pasadena, CA USA